DDC11xEVM-PDK User's Guide

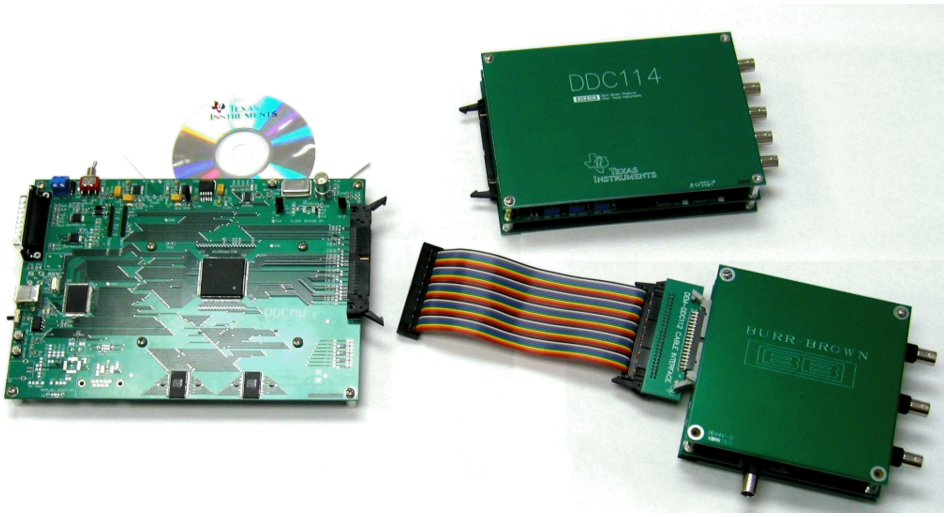

Figure 1. DDC11xEVM-PDK Photo

The DDC11xEVM-PDK is an evaluation kit for evaluating the DDC112 (dual channel) and DDC114 (quad channel) current input 20-bit analog-to-digital (A/D) converters. The kit consists of a motherboard (DDCMB) for interfacing to a PC, one DDC112 device board (DEM-DDC112U-C), and one DDC114 device board (DDC114EVM). Easy-to-use software for the Microsoft Windows® operating system is included that allows performance evaluation of either device. Complete circuit descriptions, schematic diagrams, and bills of material are included in this user's guide.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Table 1. EVM-Compatible Device Data Sheets

DEVICE	LITERATURE NUMBER
DDC112U	SBAS085
DDC114	SBAS255
OPA350	SBOS099
SN74HC125	SCLS104
SN74HCT244	SCLS175
SN74HCT541	SCLS306
SN74LVC07	SCES337
TPS75225	SLVS242
TPS75233	SLVS242
UC282-ADJ	SLUS317
TUSB3410	SLLS519
MAX3221	SLLS348

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1 Introduction

The DDC11xEVM-PDK provides an easy-to-use platform for evaluating the DDC112 or DDC114 charge digitizing A/D converters. A PC interface board (DDCMB) and daughterboards for the DDC112 or DDC114 are included along with software that makes analysis and testing of these devices simple.

2 DDC112

The DDC112 is a dual input, precision, wide dynamic range, charge digitizing A/D converter with 20-bit resolution. The functional block diagram is shown in Figure 2. Low-level current output devices, such as photosensors, can be directly connected to the DDC112 input. The most stringent accuracy requirements of many unipolar output sensor applications occur at low signal levels. The DDC112 combines the functions of current-to-voltage conversion, integration, programmable full-scale, A/D conversion, and digital filtering to produce precision, wide dynamic range results. Oversampling and digital filtering reduce system noise dramatically. Correlated double sampling captures and eliminates steady state and conversion cycle-dependent offset and switching errors that conventional analog circuits do not eliminate.

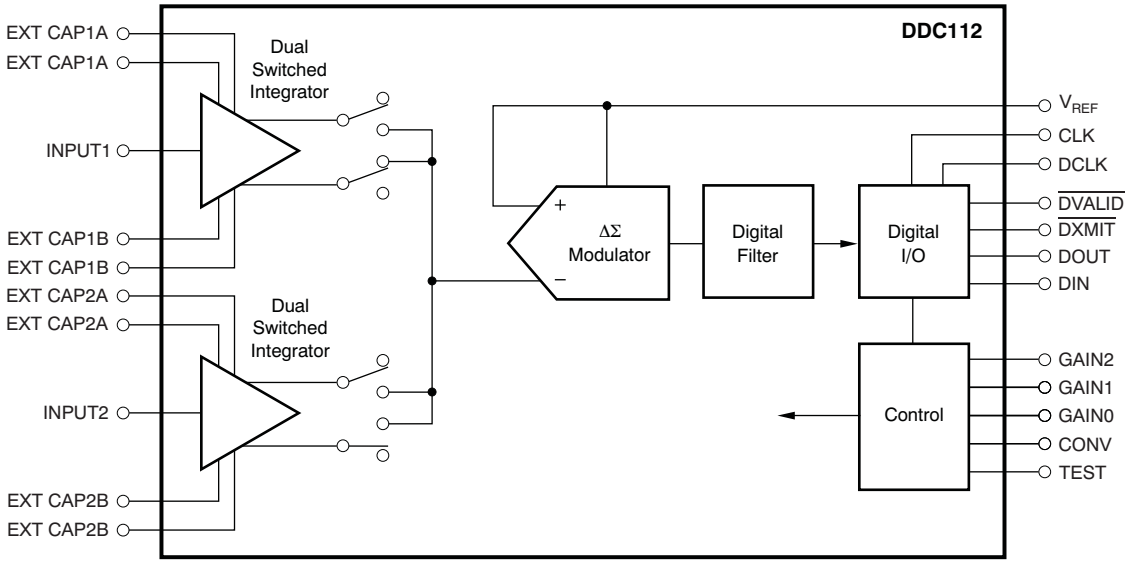


Figure 2. DDC112 Functional Block Diagram

The DDC112 continuously integrates the input signal by incorporating one dual integrator (A and B) per input channel. The output of the dual integrators are multiplexed into the A/D converter. In operation, one side of each input integrates the input charge, while the other side is being converted by the delta-sigma A/D converter and then reset. Figure 3 illustrates this operation. Another unique feature of the DDC112 is the option of external integrating capacitors. This option allows a user-programmable full-scale range. On the DEM-DDC112U-C evaluation fixture, sockets are provided on the device under test (DUT) board (E_{13} to E_{20}) to allow for easy insertion of these optional capacitors.

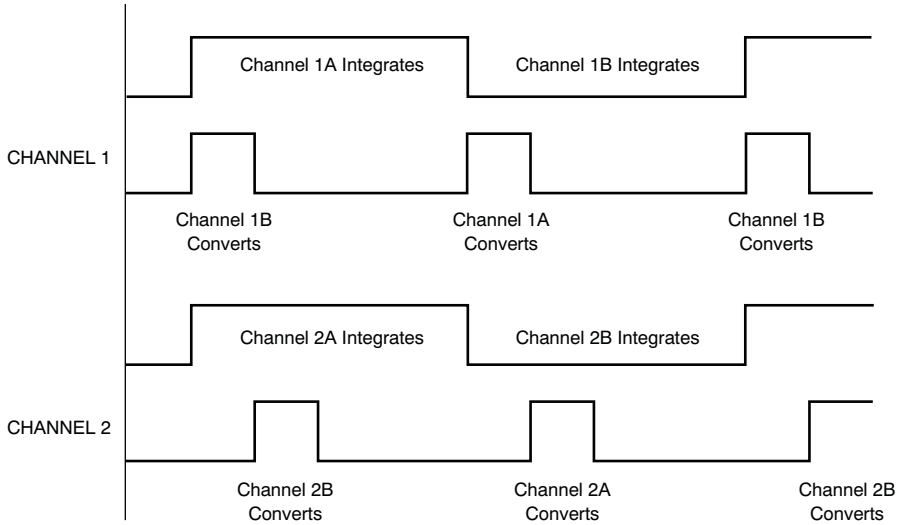


Figure 3. Integration/Conversion Timing of a Dual DDC112 A/D Converter

The gain of the DDC112 can be programmed to seven predetermined values through the software. Likewise, a user can install four external capacitors (C9, C10, C11, and C12) and design in a custom gain setting. Table 2 summarizes the available gain options.

Table 2. Input Ranges vs Gain Settings for the DDC112[(1)]

INPUT RANGE Q_{IN} RANGE (pC)	INTEGRATION CAPACITOR (Nominal) C_{INT} (pF)
–0.2 to 50	12.5 (internal)
–0.4 to 100	25.0 (internal)
–0.6 to 150	37.5 (internal)
–0.8 to 200	50.0 (internal)
–1.0 to 250	62.5 (internal)
–1.2 to 300	75.0 (internal)
–1.4 to 350	87.5 (internal)
–4.0 to 1000	250 (external)

(1) In this example, the integration time is 1 ms.

Assuming a 10MHz system clock (pin 10 of the DUT), the relationship between the integration time, input current, and input charge is summarized in Equation 1 through Equation 3.

$$T_{INT} = \frac{Q_{IN}}{I_{IN(max)}} \quad (1)$$

$$\left(\frac{T_{INT}}{C_{INT}}\right) = \left(\frac{V_{REF}}{I_{IN(max)}}\right) \quad (2)$$

$$C_{INT} = \left(\frac{Q_{IN}}{V_{REF} - 0.1V}\right) \quad (3)$$

where

- T_{INT} = integration time in ms
- Q_{IN} = input charge in coloumbs
- I_{IN} = input current in amperes

The dual switched integrators of the A/D converter use a differential input topology, with the noninverting input internally tied to VREF. This architecure allows the digitizer to operate from a single supply. Before the beginning of each integration, the integrator is reset to VREF. Additionally, the offset, offset drift, noise, and kT/C errors are corrected at that time. A low-noise voltage reference of 4.096V (nominal) provides the best performance from the DDC112. The reference that is designed for the DEM-DDC112U-C DUT board is implemented with a LM4040 (4.1V reference), a low-pass R/C filter, and a single-supply operational amplifier (U3). The operational amplifier is loaded with multiple capacitors in an effort to further reduce reference noise and ripple.

A digital filter in the DDC112 passes a low-noise, high-resolution digital output to the serial I/O register. Because the serial I/O register is independent of the DDC112 conversion process, the output of multiple DDC112 units can be connected together in series to minimize interconnections.

The DDC112 integrates on one side of the dual switched integrator while it digitizes the other side (as illustrated in Figure 3). In the event that the integration time is less than the amount of time required to digitize Channel 1 and Channel 2, the DDC112 changes to a non-continuous mode. In this mode, the integration is not continuous and the device appears to skip integrations. The limiting factor in these situations is the time required to digitize the signals (Channel 1 and Channel 2).

3 DEM-DDC112U-C Hardware Description

The DEM-DDC112U-C is a device-under-test (DUT) board that contains a socket for one DDC112 device to be tested, data buffers, 4.1V reference, decoupling capacitors, sockets for optional input circuits, sockets for optional external gain configurations, and an analog breadboard area (see Figure 26 for circuit diagram and Figure 27 through Figure 29 for layout artwork).

The DUT socket (as shown in Figure 4) has been selected to allow for easy evaluation of multiple DDC112U devices for part-to-part comparison as well as easy onboard performance evaluation. Multiple parts can be evaluated by removing and reseating the socket frame. The socket frame is easily removed by gently dislodging either end with needle-nose pliers, a very small slotted screwdriver, or tweezers. Once one end of the socket frame has been lifted, the entire frame can be removed by lifting the other end. To reinstall the frame, place the DDC112U on top of the socket. Slide one end of the frame in first, and then push the other side to snap into place. Alternatively, push down on both ends evenly, until the socket frame snaps into place. Then make sure the pins are aligned properly. Place the socket frame over the socket, carefully aligning it with the socket underneath. Repeated removal of the socket frame may damage the frame. Contact Robinson-Nugent for replacement frames.

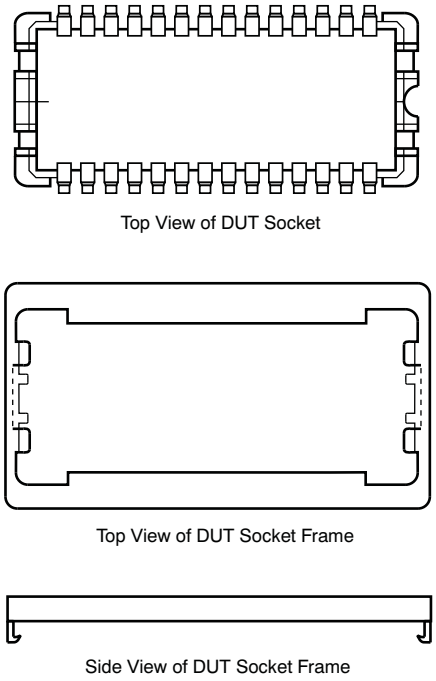


Figure 4. Robinson-Nugent Socket for DUT

This unique socket was also selected to allow onboard performance evaluations. This type of evaluation can be done by desoldering the socket and soldering a DDC112U directly to the board. To enable this method, the socket frame must be removed before desoldering the socket. Caution should be exercised with this technique because the solder mask degrades with every cycle of soldering and desoldering.

The PC interface board (DDCMB) and the DUT board are separate to minimize digital noise effects on the DDC112 unit being tested, as well as to allow for other DUT boards to be used (for example, a board with multiple converters). Digital buffers are installed at both ends of the interface to improve the isolation between the boards. The DEM-DDC112U-C board is attached to the DDCMB using the DEM-DDC112 Cable Interface that snaps into P1, and a cable that connects from the Cable Interface board to the DDCMB.

The DEM-DDC112U-C DUT board is carefully laid out to ensure low-noise evaluations. Note that all the digital pins are located on one end of the DDC112U with the analog pins on the other. Be careful to keep the digital activity as far away from the analog pins as possible. In particular, pins 9 through 17 of the DDC112U have higher digital activity than the others, and should be shielded from the analog functions. The digital return lines are carefully separated on the DEM-DDC112U-C DUT board. The additional ground plane shields on the top and bottom of the DEM-DDC112U-C DUT board are installed with the board to ensure that low-noise tests are possible. During operation, the lid of the DEM-DDC112U-C DUT board should be closed.

Proper grounding and shielding practices should be taken into consideration when designing the circuit layout for the DDC112. In the event that the application cannot tolerate the additional shields of the DEM-DDC112U-C DUT board, an alternative layout is shown in Figure 5, where a PC ground plane is placed around the inputs of the DDC112 (pins 1 and 28). This shield helps minimize coupled noise into the input pins. Additionally, the pins that are used for the external integration capacitors (pins 3, 4, 5, 6, 23, 24, 25, and 26) should be guarded by a ground plane when the external capacitors are used.

The digital and analog planes are not separate on this demonstration fixture because of the low level of digital activity on the board. Regardless of the power-supply strategy, the bypass capacitors should be as close to the device as possible.

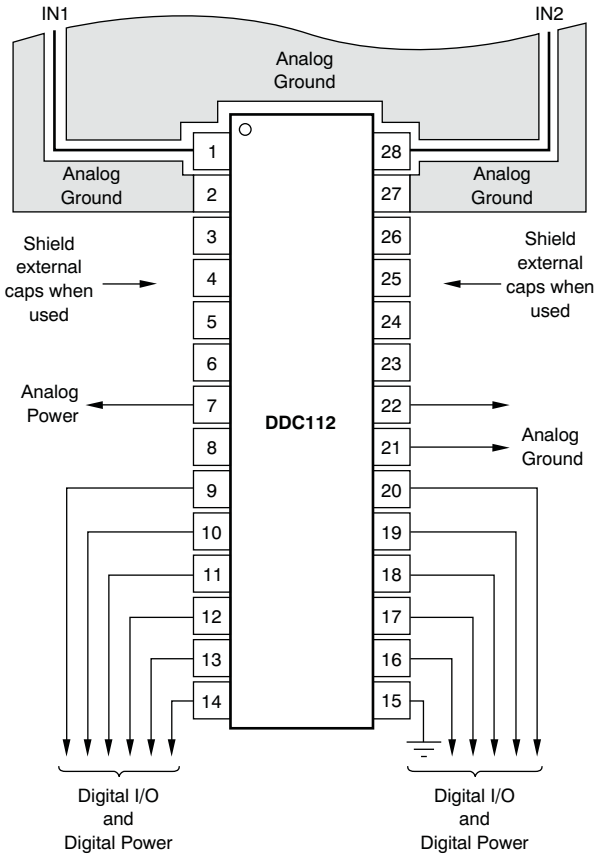


Figure 5. Recommended Shield for DDC112 Layout Design

3.1 Reference Circuit

The 4.096V reference that has been installed on the DEM-DDC112U-C DUT board has been carefully selected because of its low-noise performance. The LM4040-4.1 provides a 4.096V (nominal) reference. At the reference output, a single pole (3.157Hz) low-pass filter is inserted in the reference signal path. This filter is then followed by an amplifier configured as a buffer. The output of the amplifier has been loaded with 20.1µF of capacitance. This value of capacitance was derived through experimentation. The voltage reference circuit described above has been found to enable the DDC112U to perform optimally.

To evaluate alternative reference circuits, use jumper JP1 to connect an external reference source through the BNC connector, P5, or a user-designed reference circuit from the breadboard. Table 3 shows the jumper settings for JP1.

Table 3. Jumper Setting Definitions for JP1 for the Voltage Reference Source for the DDC112

JUMPER SETTING	JUMPER SETTING FUNCTION
Position A	Connects the 4.096V onboard reference to the DUT.
Position B	Connects the EXT VREF connector, P5, to the DUT.
Position C	Connnects the breadboard VREF bus to the DUT.

3.2 Optional Component Sockets

Resistor and capacitor sockets are included on the DEM-DDC112U-C DUT board to allow for optional input circuits and easy insertion of the optional external gain capacitors.

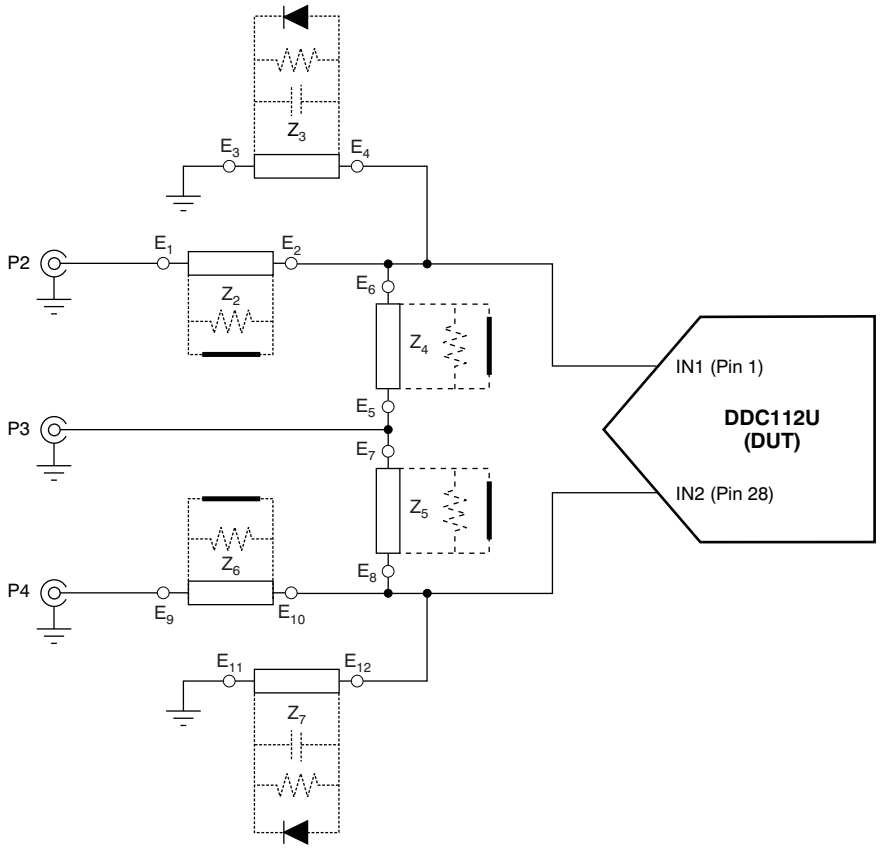


Figure 6. Input Structure on the DEM-DDC112U-C DUT Board

Figure 6 shows the topology of the input socket options and BNC connectors. With this arrangement, several different input configurations can be implemented on the DDC112 DUT board. For example, a photosensor can be installed for the IN1 (pin 1 of the DUT) using the E_3 and E_4 sockets. Alternatively, a voltage source could be used to excite the input of the converter by using P2 with a resistor installed in the Z_2 position (E_1 and E_2) sockets. Both of these configurations can be implemented on the IN2 (pin 28) input as well. A dc offset current can be injected into the input through P3. A resistor in the Z_4 position should be inserted if the source from P3 is voltage. A short should be inserted if the source is a current. It can be quickly seen that a variety of configurations can be implemented with this input circuitry configuration. The factory setting for this circuit is:

- Z_2 = 10MΩ
- Z_5 = Open
- Z_3 = Open
- Z_6 = 10MΩ
- Z_4 = Open
- Z_7 = Open

External capacitors can be inserted in the C9, C10, C11, and C12 positions, as shown in Figure 7. These external capacitors can be used to set the gain of the DDC112U (DUT) to user specifications instead of the seven internal gains available. Refer to the DDC112 portion of this user guide for more details concerning the appropriate value of these external capacitors. For further detailed information, also refer to the DDC112 product data sheet. For best performance, the leads of the capacitors should be as short as possible on C9 to C10 and C11 to C12.

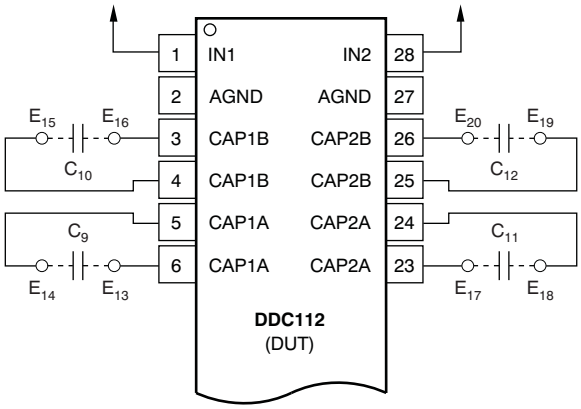


Figure 7. External Gain Capacitor Socket Configuration for the DUT Board

4 DDC114

The DDC114 is a 20-bit, quad channel, current-input A/D converter (as shown in Figure 8). It combines both current-to-voltage and A/D conversion so that four low-level current output devices, such as photodiodes, can be directly connected to its inputs and digitized.

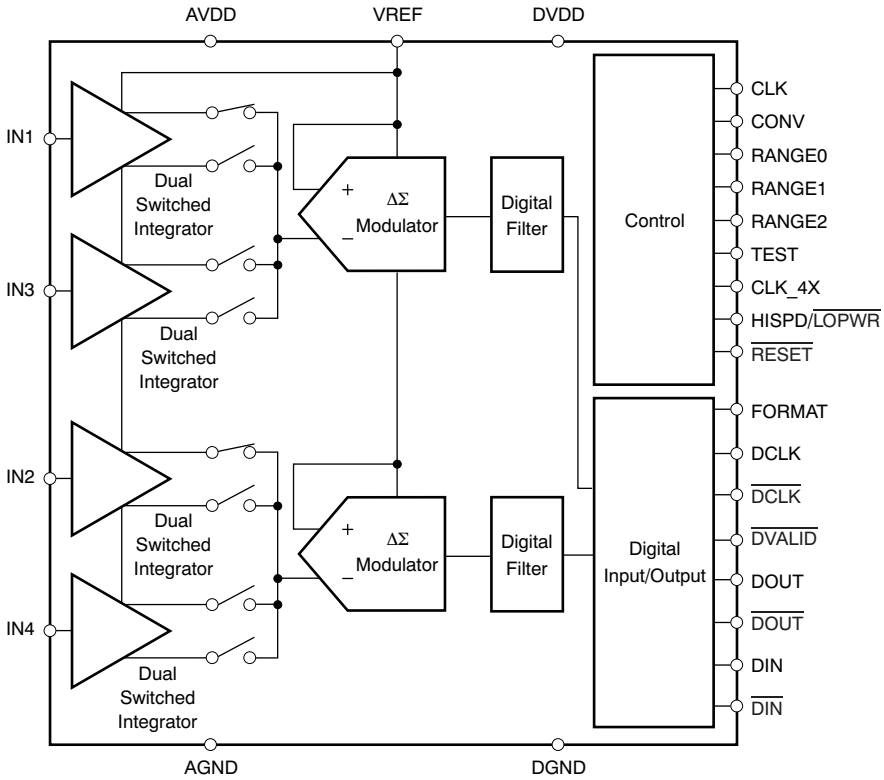


Figure 8. DDC114 Block Diagram

For each of the four inputs, the DDC114 provides a dual-switched integrator front-end. This design allows for continuous current integration: while one integrator is being digitized by the onboard A/D converter, the other is integrating the input current. Adjustable full-scale ranges from 12pC to 350pC and adjustable integration times from 50µs to 1s allow currents from fAs to µAs to be measured with outstanding precision. Low-level linearity is ±0.5ppm of the full-scale range and noise is 5.2ppm of the full-scale range.

In many ways, the DDC114 can be viewed as a dual DDC112; the difference between the devices is that the DDC112 offers the option of using external integrating capacitors, giving it the possibility for extended input ranges.

There are eight different capacitors available on-chip for both sides of every channel in the DDC114. These internal capacitors are trimmed in production to achieve the specified performance for range error of the DDC114. The range control pins (RANGE0–RANGE2) change the capacitor value for all four integrators. Consequently, all inputs and both sides of each input have the same full-scale range. Table 4 shows the capacitor value selected for each range selection.

Table 4. Range Selection of the DDC114

RANGE2	RANGE1	RANGE0	C_F (pF, typ)	INPUT RANGE (pC, typ)
0	0	0	3	–0.048 to 12
0	0	1	12.5	–0.2 to 50
0	1	0	25	–0.4 to 100
0	1	1	37.5	–0.6 to 150
1	0	0	50	–0.8 to 200
1	0	1	62.5	–0.1 to 250
1	1	0	75	–1.2 to 300
1	1	1	87.5	–1.4 to 350

5 DDC114EVM Hardware Description

The DDC114EVM is a device-under-test (DUT) board with a DDC114 device, data buffers, and a 4.1V reference (see Figure 34 for circuit diagram and Figure 36 through Figure 38 for layout artwork). The interface and the appropriate circuit options for this device are similar to those available on the DUT board for the DDC112.

Three power-supply connections are provided on this DUT board: 5V, DVDD, and AVDD. The 5V supply is regulated on the DUT board to provide a 3.3V supply for the interface buffers. DVDD is the digital supply for the DDC114 and can range from 2.7V to 5.5V; AVDD is the analog supply to the DDC114 and must be between 4.75V and 5.25V. Jumpers J6 and J16 allow the board 5V and AVDD supplies to be tied to DVDD, if a single 5V supply is used. Table 5 summarizes the powering options of this board.

Table 5. Power Option Jumpers for DDC114 DUT Board

JUMPER	DESCRIPTION
J6	When installed, 5V is connected to DVDD (J18). When not installed, 5V must be supplied through J17.
J16	When installed, AVDD is connected to DVDD (J18). When not installed, AVDD must be supplied through J19.

The inputs to the DDC114 device can be provided individually on the J25–J28 (AIN1 to AIN4) BNC connectors. For testing purposes, all four channels can be driven with the same signal if it is provided on J24 (AINCOM). Pin sockets are provided at each BNC connector to allow a resistor or jumper to connect the BNC to the actual input channel. Refer to the schematic (see Figure 34) for details. The factory settings for this circuit is summarized in Table 6:

Table 6. DDC114 DUT Board Circuit Factory-Enabled Settings

CHANNEL				
1	R7 = 10MΩ	R8 = Open	R9 = Open	J20 = GND
2	R10 = 10MΩ	R11 = Open	R12 = Open	J21 = GND
3	R15 = 10MΩ	R16 = Open	R17 = Open	J22 = GND
4	R18 = 10MΩ	R19 = Open	R20 = Open	J23 = GND

This configuration brings in one signal on AINCOM (J24) that feeds all four channels through an individual 10MΩ resistor per channel.

6 DDCMB Hardware Description

The PC interface board, or motherboard, is called the DDCMB. This board has a USB interface for connecting to a PC; the USB interfaces to a small microcontroller that controls the functions of a Xilinx Spartan™-3 FPGA. The FPGA generates all the timing signals that are sent to the DUT and handles communication of data between the DUT and the PC.

The DDCMB is designed to be extremely flexible and therefore has many configurable settings. These settings are described in the following subsections. When using the board with this evaluation kit, the default settings should be used. Refer to the schematic diagram in Figure 39.

6.1 Motherboard Connectors

The USB interface to a personal computer is provided on J3. The connection to a DUT daughtercard is made using the J13 50-pin header.

Some connectors are only provided for use in manufacturing the DDCMB. J8 and J9 are JTAG and FPGA headers for configuration of the FPGA. Alternately, the EEPROM and FPGA can be programmed using the J1 parallel port connection.

Power is supplied to the DDCMB through J12. This input should be +5VDC.

J17 can be used to monitor the FPGA clock or as an external clock input. If supplying a clock through J17 to the board, the onboard crystal oscillator, U7, must be desoldered and removed.

6.2 Motherboard Jumpers

Refer to Figure 42 for location of jumpers on the DDCMB.

6.2.1 Clock Options

Two clocks are used on the DDCMB: a clock for the USB microcontroller, and a clock for the FPGA. The FPGA generates all clocking signals for the DUT daughtercards. While jumpers are provided for a number of clocking options, the DDCMB is populated only with the circuitry to support using the onboard crystal oscillators and without provision for clock division. For the sake of completeness, however, refer to Table 7 for the possible jumper settings. These jumpers should remain in the default positions.

Table 7. Clock Option Jumpers

JUMPER	FUNCTION	OPTIONS	DEFAULT
J4	USB Microprocessor Clock Source	Not Installed;Use X1 (24MHz onboard crystal) 1-2: Use external clock provided on J6 2-3: Use U25 crystal oscillator Note: J4, J6, and U25 are not populated on the DDCMB	Not Installed
J7	FPGA Clock Source	USB_uC and the center post; USB Microprocessor Clock J7 center pin and EXT: U7 provides 80MHz clock /BY and CLK: clock divider circuit through J14.	Center post to EXT.
J14	Clock Divisiion Ratio	/2: Divides the clock frequency by two /4: Divides the clock frequency by four /8: Divides clock frequency by eight Not installed: no clock division	Not Installed

6.2.2 Power Supplies

Jumpers are provided for supplying power to the FPGA. These jumpers should be left installed unless one wishes to make current measurements of the FPGA supply currents. J21 provides 3.3V to the daughtercard via the 50-pin connector; if this option is used, assure that the daughtercard is not also supplying 3.3V locally.

Table 8. Power Supply Jumpers

JUMPER	SUPPLY FUNCTION	DESCRIPTION	DEFAULT SETTING
J10	FPGA 3.3V	This connects the 3.3V regulated supply to the FPGA I/O pin supplies for all the I/O banks. It also powers the IL71x isolators, and the FPGA side of TI parallel port buffer/driver 74LVC161284.	Installed
J11	FPGA 1.2V	This connects the 1.2V regulated supply to the FPGA core supply	Installed
J18	FPGA 2.5V	This connects the 2.5V regulated supply to the FPGA core supply	Installed
J21	DUT 3.3V	Provides the 3.3V power supply across the 50-pin header to the daughter cards if connected	Installed

6.3 Motherboard Switches

The DDCMB has a master power switch, S5, marked *MSTR* on the board. This switch should be set to the ON position whenever the DDCMB is used.

S1 is the EEPROM selector for the USB microcontroller and must always be set to the GND position.

S3, WAKEUP, wakes up the USB controller from sleep mode. Normally, it should not be necessary to use this switch.

S4, RESET_USB, resets the USB controller. Pushing this switch may be necessary if the DDCMB is not recognized by your PC when connecting it to the DDCMB.

S8, RESET_FPGA, resets the FPGA. Normally, it should not be necessary to use this switch.

6.4 Hardware LEDs on the Motherboard

A number of LED indicators are on the DDCMB. These indicators allow ease of monitoring the state the motherboard is in. Refer to Table 97 for a summary of these indicators.

Table 9. DDCMB LED Indicator Functions

LED	Function Indicator
D1	USB bus power detected.
D8	FPGA configuration is done.
D7	The motherboard is powered on.
D9	J10 is providing 3.3V power to motherboard.
D10	J18 is providing 2.5V power to motherboard.
D12	The FPGA is powered on.
D11	3.3V motherboard to daughterboard power is connected.

7 DDC11xEVM-PDK Kit Operation

This section provides information on using the DDC11xEVM-PDK, including setup, program installation, and program usage.

7.1 Minimum Requirements

Before installing the software please verify that the PC meets the following minimum requirements:

- Microsoft Windows XP® operating system with Service Pack 2 (SP2) installed
- 1024 x 768 screen resolution
- USB 2.0 compatible port

Other configurations may work; however, they are not tested. Users should be advised that when capturing larger data sets, PCs equipped with the faster processors and ample memory tend to perform best.

7.2 Installing the Software

Before installing the DDC11xEVM-PDK application software, the USB drivers must be installed. This step is best accomplished by inserting the CD-ROM into the PC and letting Windows find the drivers when the hardware connects. The drivers are located in the driver directory on the CD. To begin, connect a 5V power supply to J12 on the DDCMB, and turn on the MSTR power switch. Connect a USB cable from the computer to the DDCMB through J3.

Use the Windows *Found New Hardware* Wizard to install the drivers. The DDCMB requires a boot driver and an application driver; therefore, new setups require going through the Found New Hardware Wizard twice. Figure 9 through Figure 14 show the first driver screens that appear.

Figure 9. Initial Found New Hardware Wizard Screen

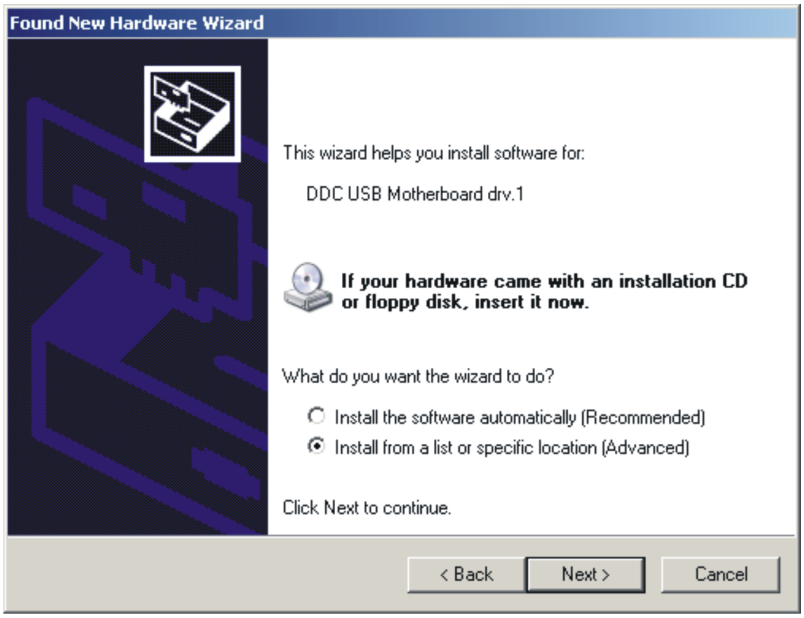


Figure 10. Driver Selection for DDC USB Motherboard drv.1

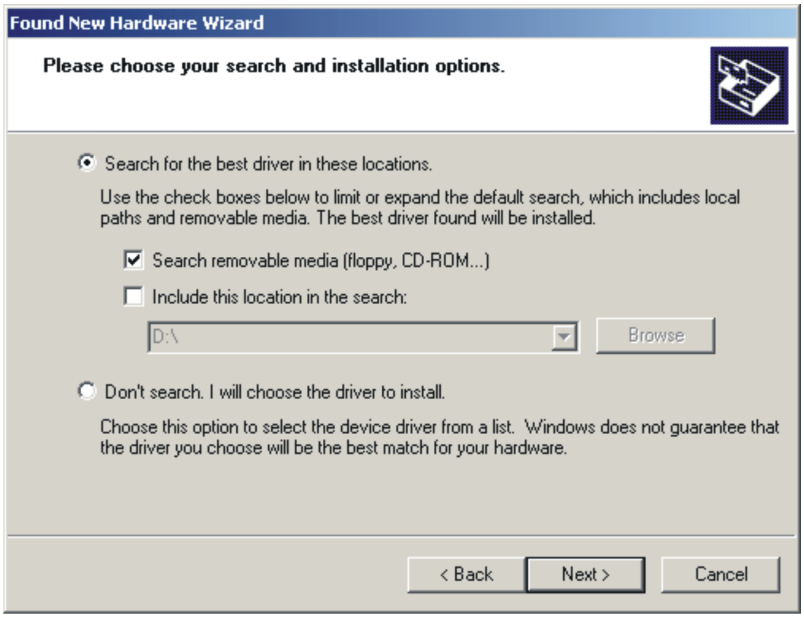


Figure 11. Select to Search Removable Media to Find Drivers on CD

Note: You may see notices (Figure 12) that the drivers are not digitally signed, and given the option to accept the drivers anyway. Choose *Continue Anyway*.

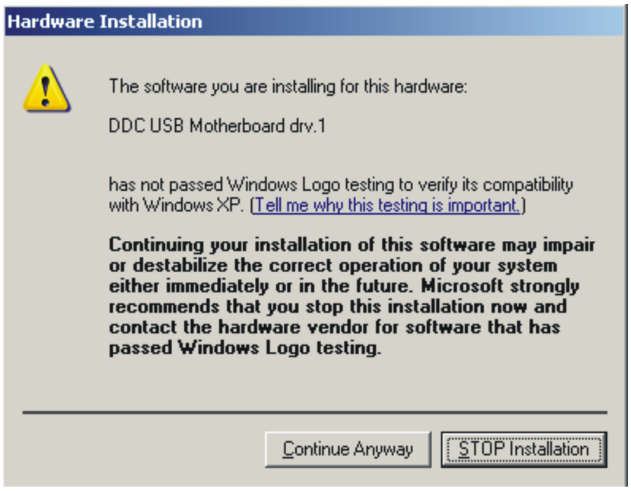


Figure 12. Driver Not Signed Notification—Choose Continue Anyway

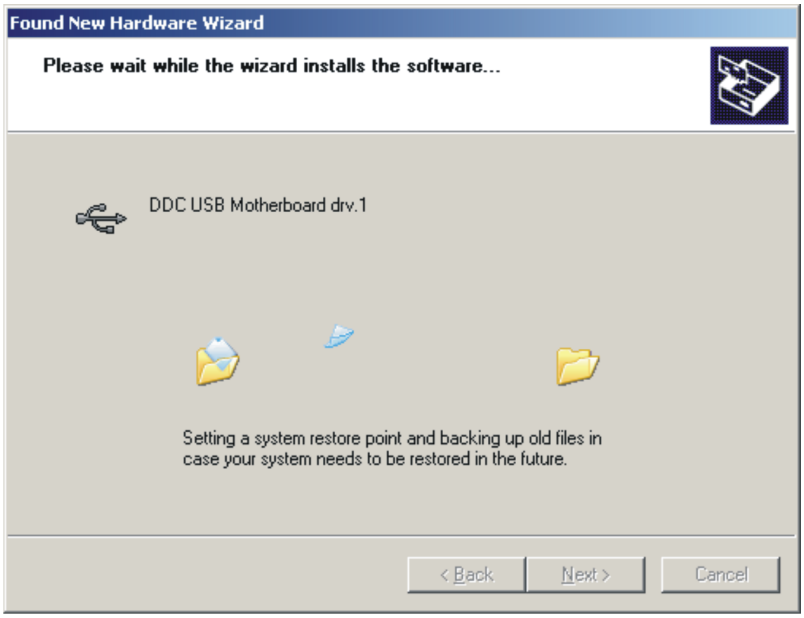


Figure 13. Copying Driver Files

Figure 14. First Driver Installation Complete

After the first driver is installed, disconnect and reconnect the USB cable to the DDCMB, or press the RESET_USB button on the DDCMB. This step causes the second driver to be installed. You will then see screens similar to those in Figure 15 through Figure 17.

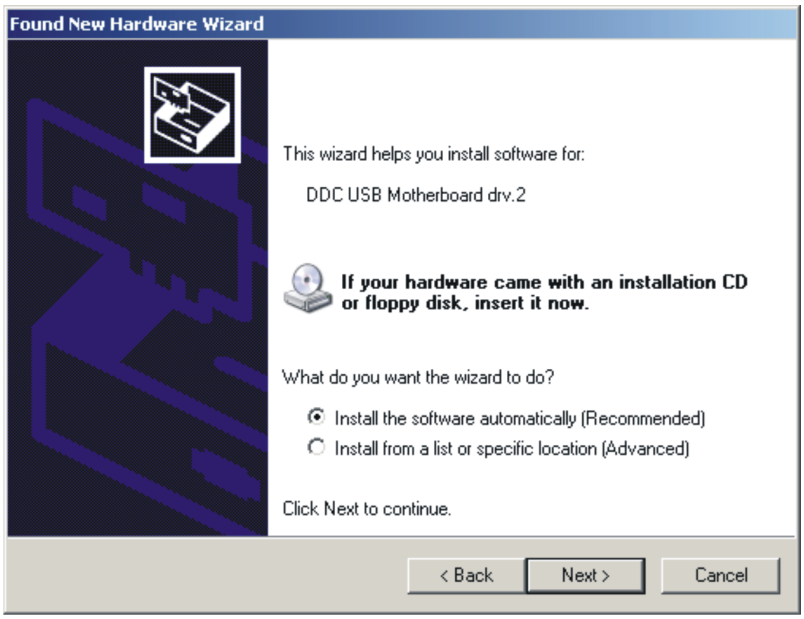


Figure 15. Driver Selection for DDC USB Motherboard drv.2

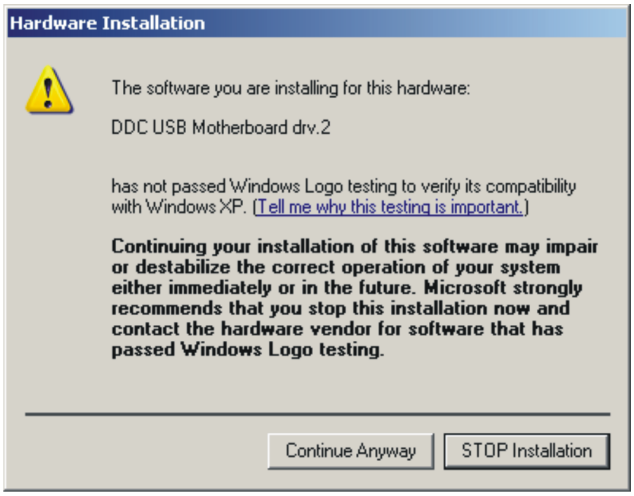


Figure 16. Second Driver Not Signed Notification—Choose Continue Anyway

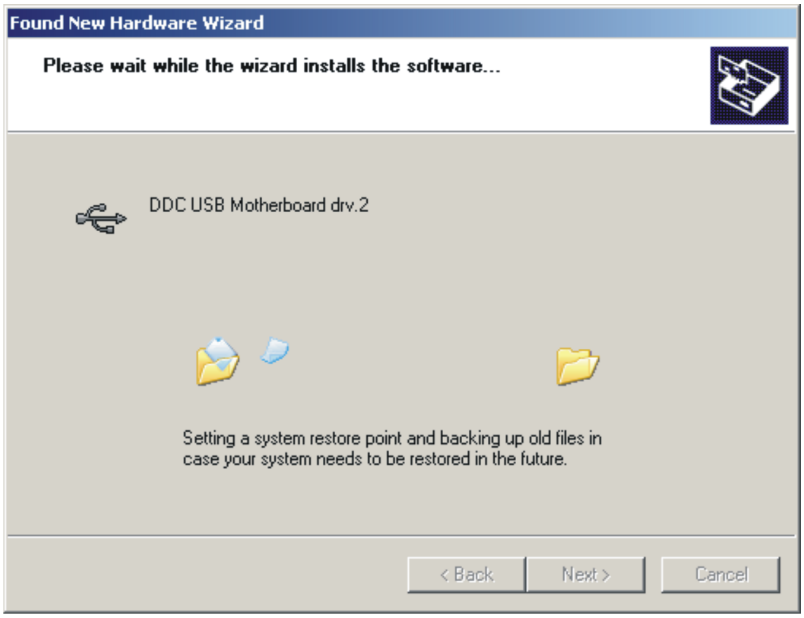


Figure 17. Copying Files for Additional Driver

Once the USB drivers are installed, the DDC11x Evaluation program can be installed. Double-click on setup.exe in the install directory. A screen similar to that shown in Figure 18 appears.

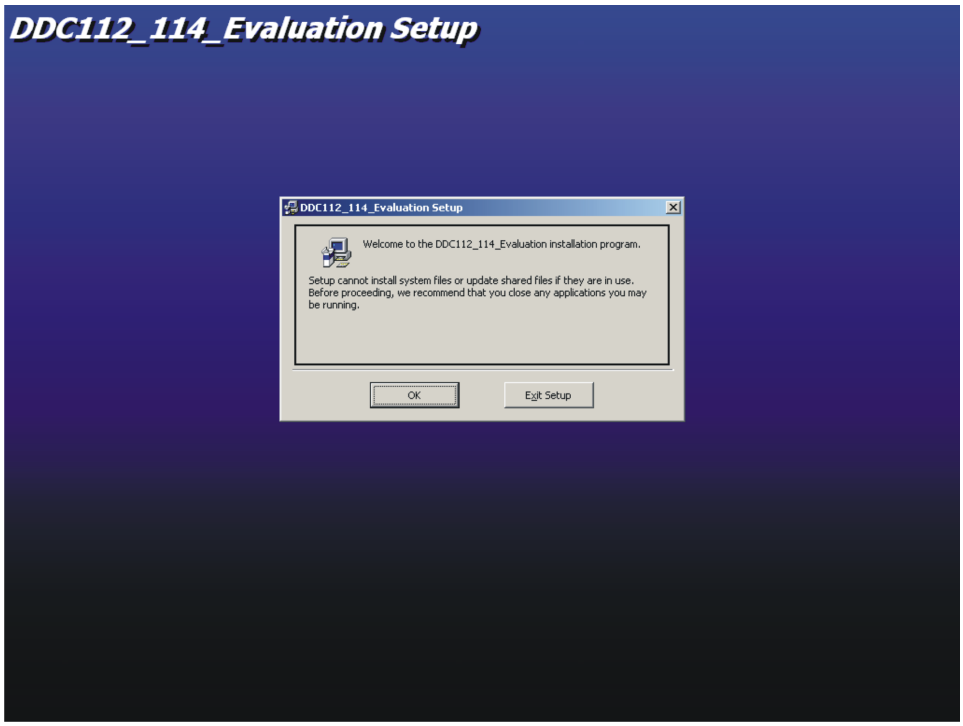


Figure 18. Initial Software Installer Screen

Next, the screen shown in Figure 19 appears. Verify that the installation directory is correct, and press the large button in the upper left corner of this screen to proceed.

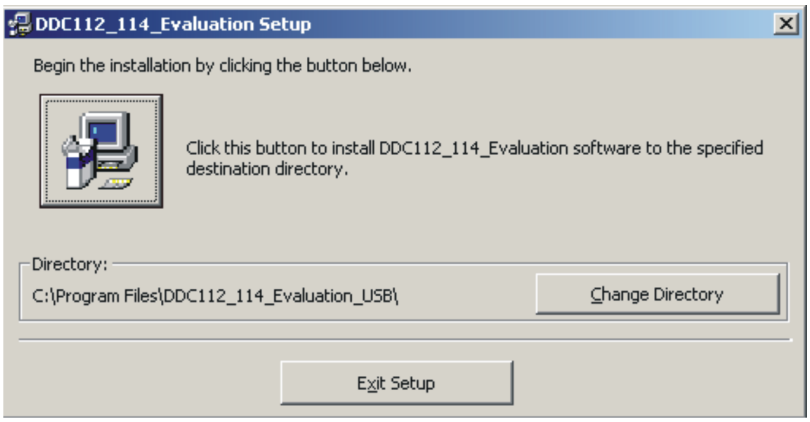


Figure 19. Choose Software Installation Directory

When the installer completes copying files, the screen shown in Figure 20 appears.

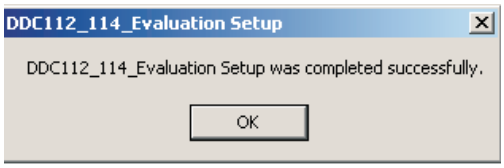


Figure 20. Software Installation Complete

The software installation is now complete. Disconnect power from the DDCMB and proceed to the next section.

7.3 Evaluating a DDC11x Device: Quick Start

With power disconnected to the DDCMB, connect one of the daughtercards to the motherboard using the supplied 50-pin ribbon cable. If connecting the DEM-DDC112U-C, the DEM-DDC112 Cable Interface adapter board must be used to attach the cable to the daughterboard. This adapter is not needed when connecting the DDC114EVM daughterboard.

Connect the +5VDC power supply to the DDCMB (if not connected) and daughterboard (J6 on the DEM-DDC112U-C; J17 on the DDC114EVM, assuming that jumpers J6 and J16 are installed). Turn on the +5VDC power supply.

From the Windows **Start** menu, select the *DDC112_114_Evaluation* program. The program starts and displays a window as shown in Figure 21.

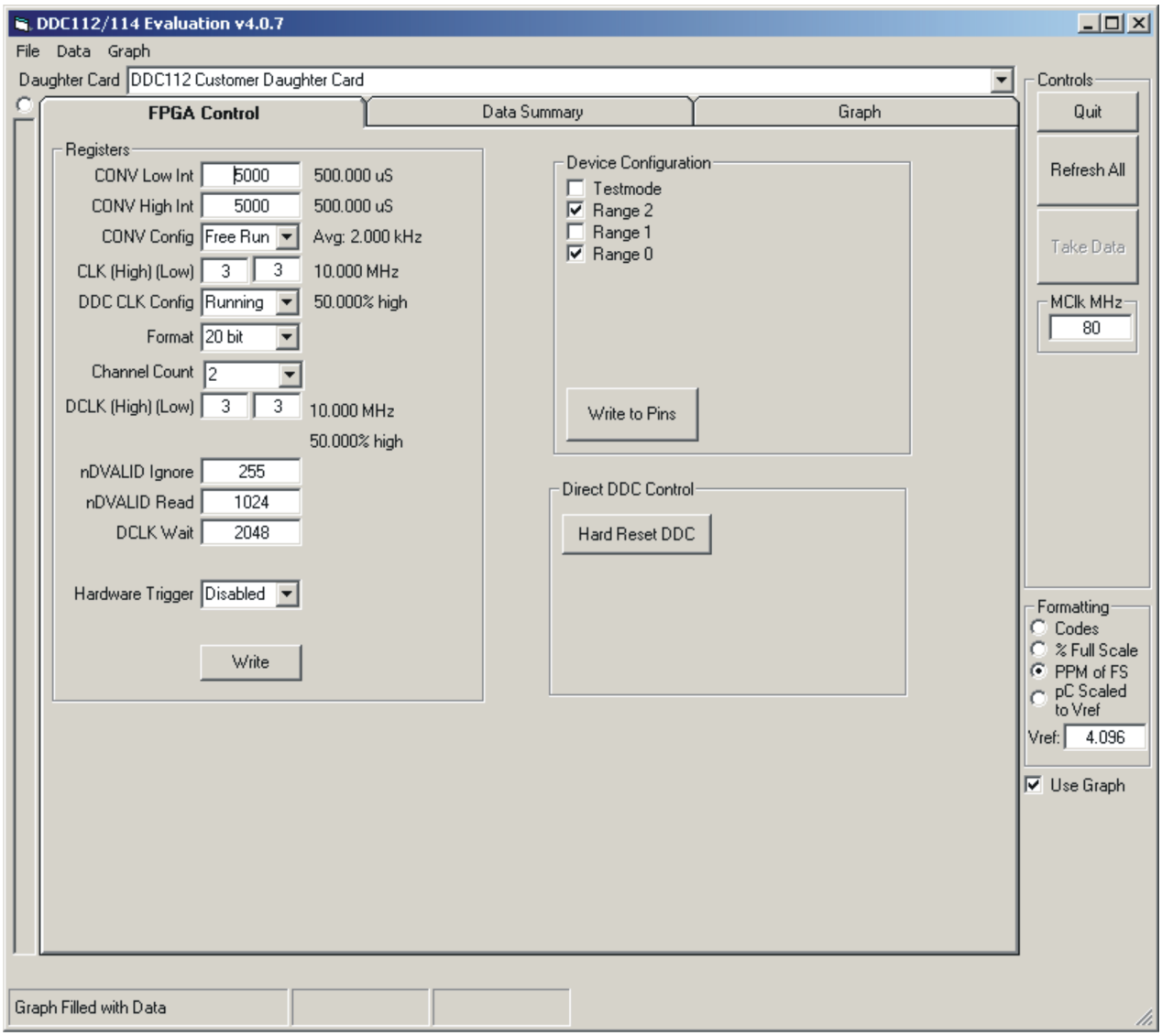


Figure 21. Initial Software Screen, FPGA Control Tab

From the **Daughtercard** drop-down menu at the top of this screen (Figure 22), select the daughtercard that is attached to the DDCMB. The settings shown on the **FPGA Control** tab are populated with the appropriate settings for the device connected.

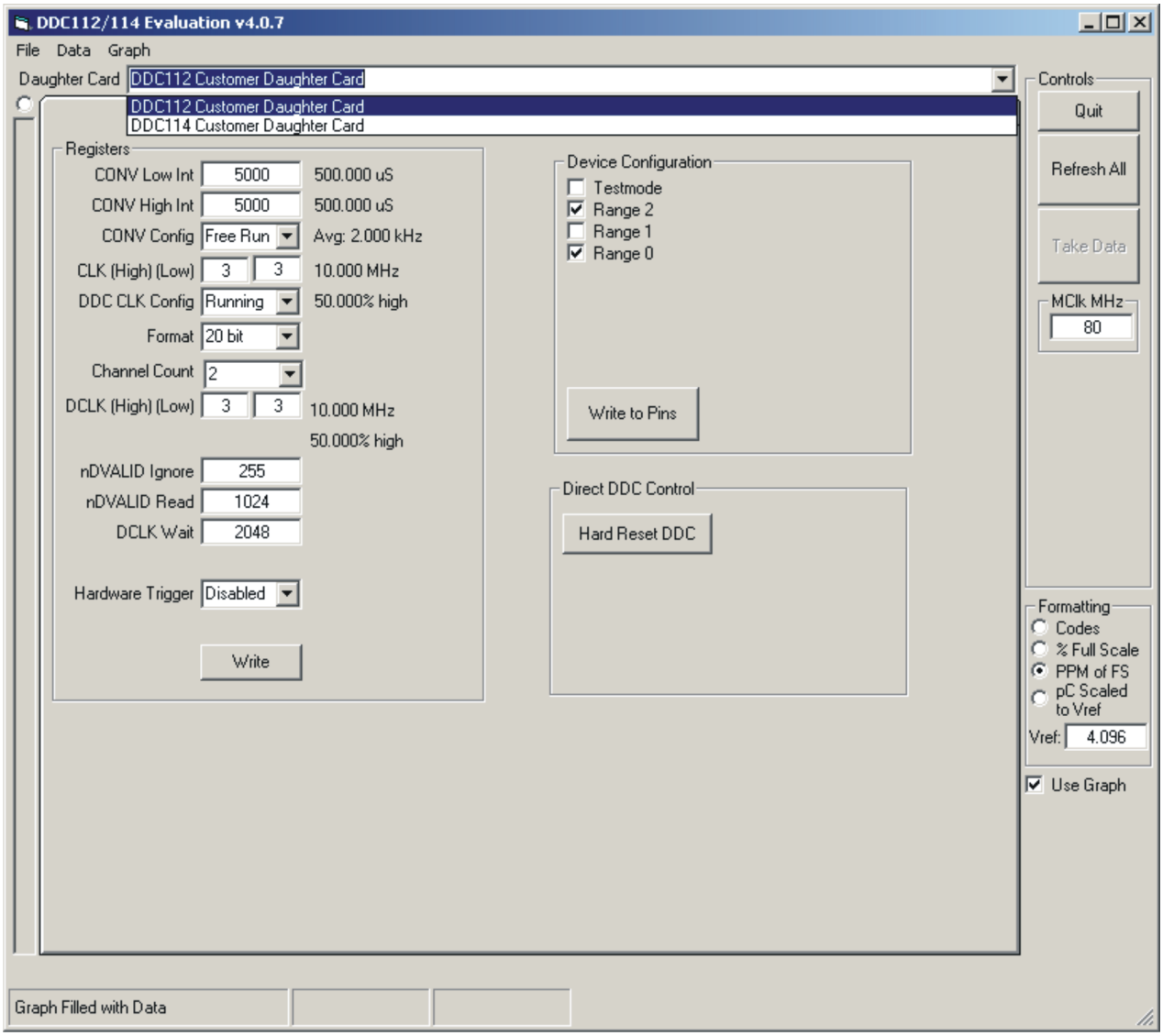


Figure 22. Daughtercard Selection

Next, do a system refresh of the FPGA by clicking on the **Refresh All** button, located in the upper right corner of this screen. This refresh initializes the system to working defaults, and verifies communication with the FPGA. When communication is established, the **Take Data** button is enabled. The software is now ready to receive data from the DDC.

7.3.1 Main Window Controls

A number of controls are always visible, regardless of the tab is selected in the main tab control.

The **Quit** button causes the program to exit and releases system resources. The **Refresh All** button updates the state of all FPGA registers and pins to those states set in the FPGA control tab. The **Take Data** button causes an acquisition cycle to occur and loads data into the program memory and will update the graph with the data if the **Use Graph** check box is checked.

Data can be displayed in a number of formats, selected with the **Formatting** controls. The options are:

- *Codes*: data are displayed in raw codes or counts
- *% Full Scale*: data are displayed as a percentage of the full scale range
- *PPM of FS*: data are displayed in units of parts per million (PPM) of the full scale range
- *pC Scaled to Vref*: data are displayed in picocoulombs

The reference voltage can be set in the **Vref** text box control. The default value is 4.096V, which corresponds to the reference voltage provided by the onboard voltage references on the DDC daughtercards, but may be adjusted if a different reference voltage is used.

7.3.2 Main Window Menus

The Main window has three menus: **File**, **Data**, and **Graph**. This section describes the functions of each menu item.

File→ *Quit*

This option releases the USB port, closes all windows, and exits the software.

Data →*Save Data from Memory*

Collected data can be saved to a standard comma-separated value (CSV) formatted spreadsheet file. No header data are written to the file; only raw data. The columns are written in this order: Channel Name, Reading #, Reading [codes], Range [0-7], Vref [V], # of Bits [16 or 20].

Once a reading is made, the data can be saved to a file using the *Save Data from Memory* menu item. The data can then be analyzed further in Microsoft Excel® or a similar spreadsheet application that can parse data in user-defined CSV format.

Graph →*Plot Data on Graph*

If data are loaded into memory but not plotted on the graph (because the **Use Graph** check box is not checked), selecting this menu item plots that data on the graph.

7.3.3 FPGA Control Tab

The controls on this tab directly affect the operating mode of the DDC device being tested. This section explains the various fields and buttons that reside on this tab.

7.3.3.1 Registers Group Box

The fields in this box hold all the data that are used by the FPGA to generate the waveforms for the device under test and retrieve data. The following list summarizes of all the fields and the respective functions. Refer to the individual DDC device data sheets for further information on valid clock times and pin functions.

- **CONV Low Int**: This is the number of DDC System Clock Cycles for the CONV signal to remain low during integration. The actual time is listed next to the text box.
- **CONV High Int**: This is the number of DDC System Clock Cycles for the CONV signal to remain high during integration. The actual time is listed next to the text box.
- **CONV CONFIG**: The default value of this control is *Free Run*, and should be used in the data acquisition process. The other options should not be used.
- **CLK (High) (Low)**: This sets the high and low times of the DDC clock. The default value is 3 in both fields, representing the number of clock cycles that CLK will be high and low.

- **DDC CLK CONFIG**: Choose *Running* to enable the DDC clock or *Low* to disable the DDC clock.
- **FORMAT**: Choose how many bits wide the output word is on the DOUT line (16- or 20-bit). This option does not correspond to the FORMAT pin on the DDC114. It only controls the FPGA, and should be left at 20 bits for the DDC112 for proper operation.
- **Channel Count**: Number of channels to read back. Only the *2* or *4* settings are valid for the DDC112 or DDC114.
- **DCLK (High) (Low)**: The number of master clock cycles for DCLK to remain low and high during data readback. DCLK can be faster than the DDC System Clock, which is why DCLK is separate and may be much smaller than CLK Count.
- **nDVALID Ignore**: This is the number of nDVALID pulses to ignore, or rather the number of samples to initially discard from the device. Setting this number higher can help negate the effects of settling and give cleaner data from a dead conversion stop.
- **nDVALID Read**: This is the number of nDVALID pulses after which to capture data. The device has two sides to each integrator, so if there is a 4-channel device, 256 nDVALID Reads equate to 128 samples on four channels of both A and B sides.
- **DCLK Wait**: This is the number of master clock cycles to wait after detecting an nDVALID signal. Once a signal is detected, the data are ready; in some applications, however, a delay is helpful in acheiving desired results.
- **HARDWARE TRIGGER**: In normal operation, this should be *Disabled*. If *Enabled*, a pulse can be issued on IP_1 to start a conversion after **Take Data** is pressed. If enabled and no pulse ever comes, the program appears to be frozen. If this condition happens, disable, cancel out the error messages, and refresh.

The **Write** button sends data from the PC to the FPGA, programming the settings in the FPGA to correspond to the settings listed above. When this button is pressed, the data are written and read back. If the data read back equal the data written, the screen appears as normal; however, if the data read back is different than the data set in the fields above, the text in those fields appears in a different color than black (on most systems, it appears in a dark red color).

7.3.3.2 Device Configuration Group Box

The controls in this box set the state of device configuration bits on the selected device under test, and correspond to those pins directly.

- **Range[2:0]**: These check boxes correspond to the RANGE pins on the DDC devices, and configure the range that the DDC is in. Checked corresponds to a logic 1; unchecked is a logic 0. '000' is range 0 and '111' is range 7, etc.
- **Format**: (DDC114 only) This configures the format that the DDC114 outputs data. '1' is 20-bit data per channel; '0' is 16-bit data.
- **SPEED**: This configures the Power setting for the DDC114. Unchecked ('0') is low speed and checked ('1') is high speed.
- **Testmode**: This configures the test mode for the DDC. Unchecked ('0') turns TEST mode off, and checked ('1') is TEST mode on. TEST mode disconnects the inputs and should produce an ideal baseline for noise and offset in the system.

Pressing the **Write to Pins** button sets the corresponding device hardware pins to the states in the checkboxes.

7.3.3.3 Direct DDC Control Group Box

The **Hard Reset DDC** button applies an approximately 500ms long pulse to the nRESET pin on the DDC, resetting the device.

7.3.4 Data Summary Tab

This tab displays the data in summary form. It displays all the channels, the average value measured by the channels, the RMS noise of the measured data, the peak-to-peak noise of the measured data, and the units that all these measurements are reported in. It also displays the RMS noise of all channels averaged together at the very top left.

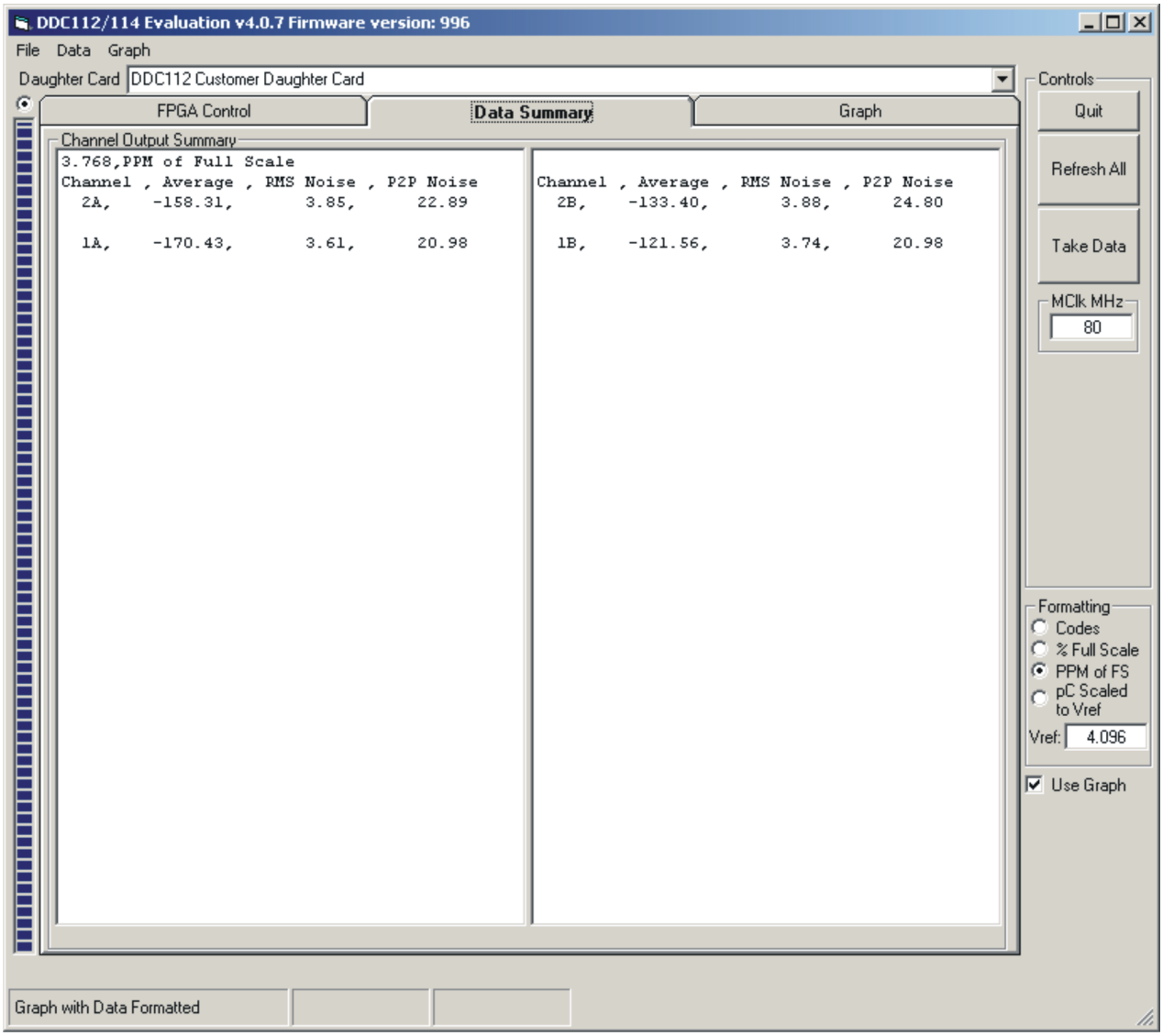


Figure 23. Data Summary Tab

The format that the data are displayed in is controlled by the formatting options set in the main window **Formatting** controls.

7.3.5 Graph Tab

The graph tab displays a graph of data versus sample acquired. It always displays the readings in codes, regardless of the **Formatting** settings. The channel to display is selected using the **Channel** combo box on the bottom of the graph.

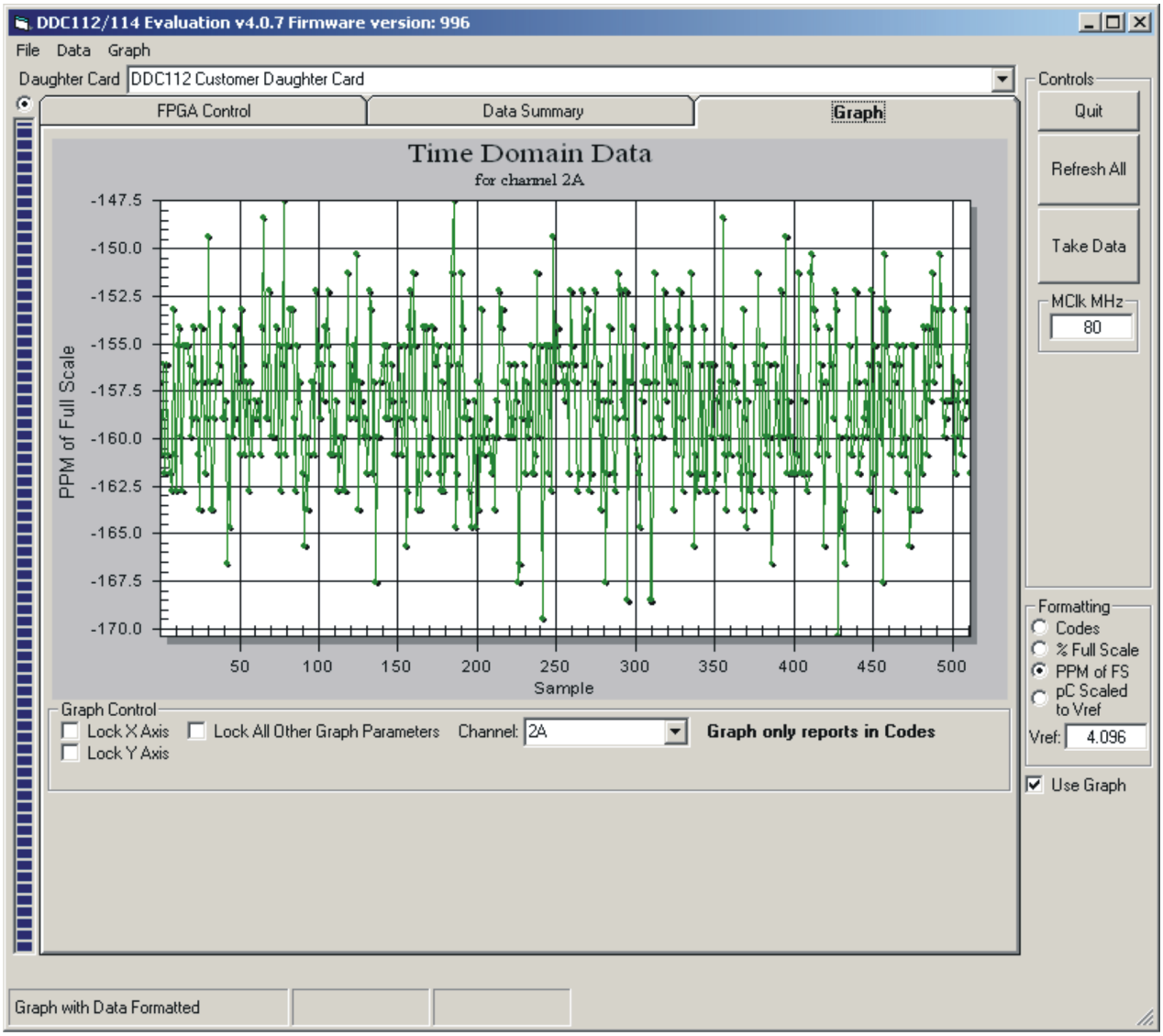


Figure 24. Graph Tab

Left-clicking and dragging a box zooms in to the selected section of the graph.

Right-clicking on the graph brings up limited zoom, format, print, and display features.

The graph zoom features can be disabled or locked using the **Lock X-axis**, **Lock Y-axis**, and **Lock All Other Graph Parameters** check boxes. These controls might be used to make it easier to zoom only horizontally or vertically without inadvertently changing the other axis.

7.4 Troubleshooting

1. If the EEPROM fails to program the FPGA when power is first applied [detectable if you cannot communicate to the DDCMB or the DONE LED (D8) does not illuminate], wait about 10 seconds for all the capacitors to charge; then toggle the MSTR power (S5) off and on again. The DONE LED should illuminate after about five seconds. If toggling the power fails to correct the problem, remove the J10 (3.3V) and J11 (2.5V) jumpers from the DDCMB board. Replace J10, wait a second, then replace J11. The board then programs.
2. If you see a dialog box as shown in Figure 25, or an error message seen on main window status bar saying *Error Writing Registers*, this message indicates that the DDCMB is either not connected via USB or has not been properly detected by the system. Verify that the USB connection is good, or press the RESET_USB (S4) button on the DDCMB to allow communication to be established.

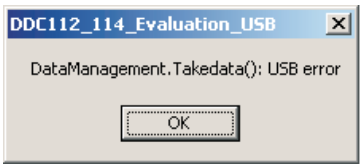


Figure 25. USB Error Notification Dialog

8 Schematics and Layout

Full-size schematics for the DEM-DDC112U-C, DEM-DDC112 Cable Interface, DDC114EVM, and DDCMB boards are appended to this user's guide. The bills of material for each board are provided in Section 8.1.

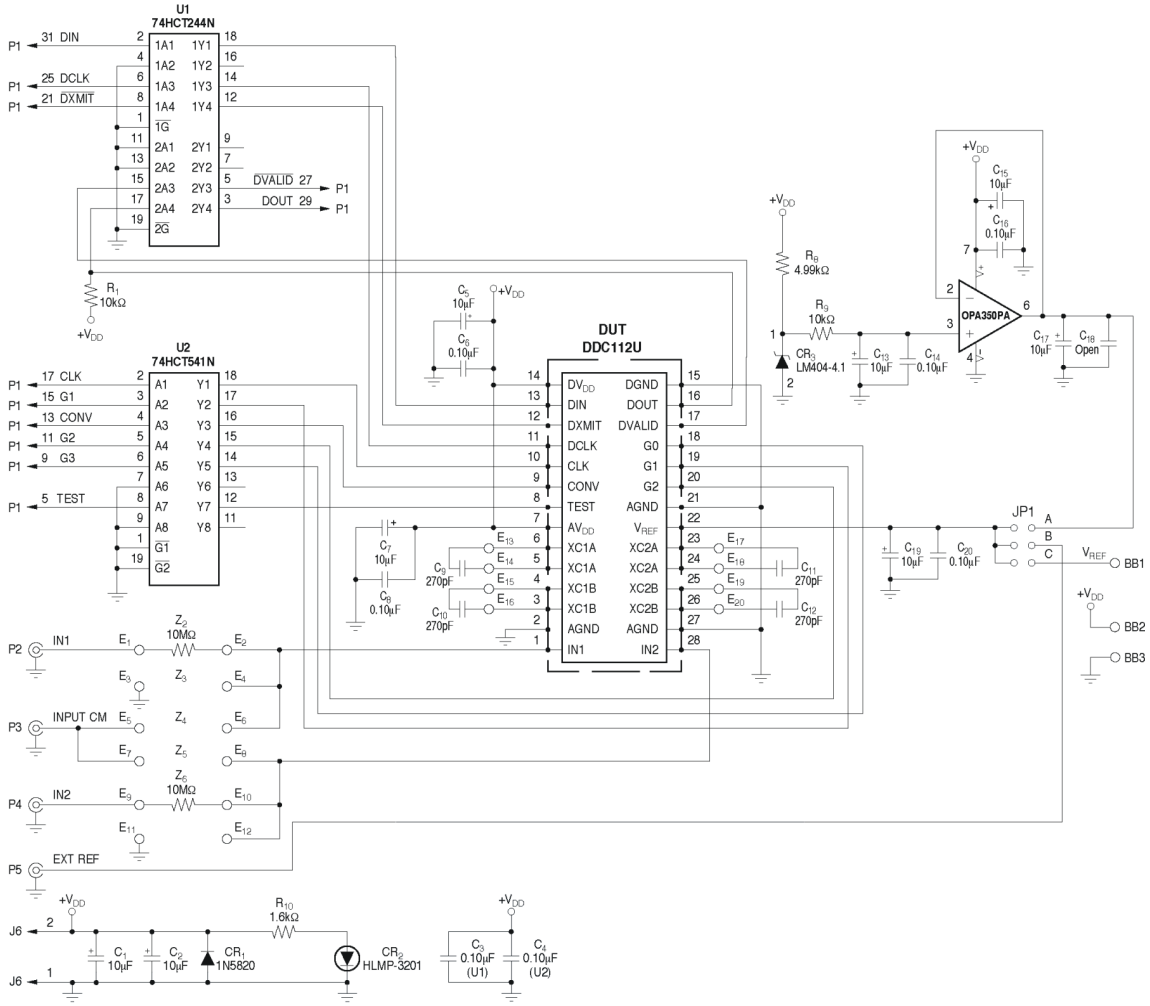


Figure 26. Schematic for DEM-DDC112U-C DUT Board

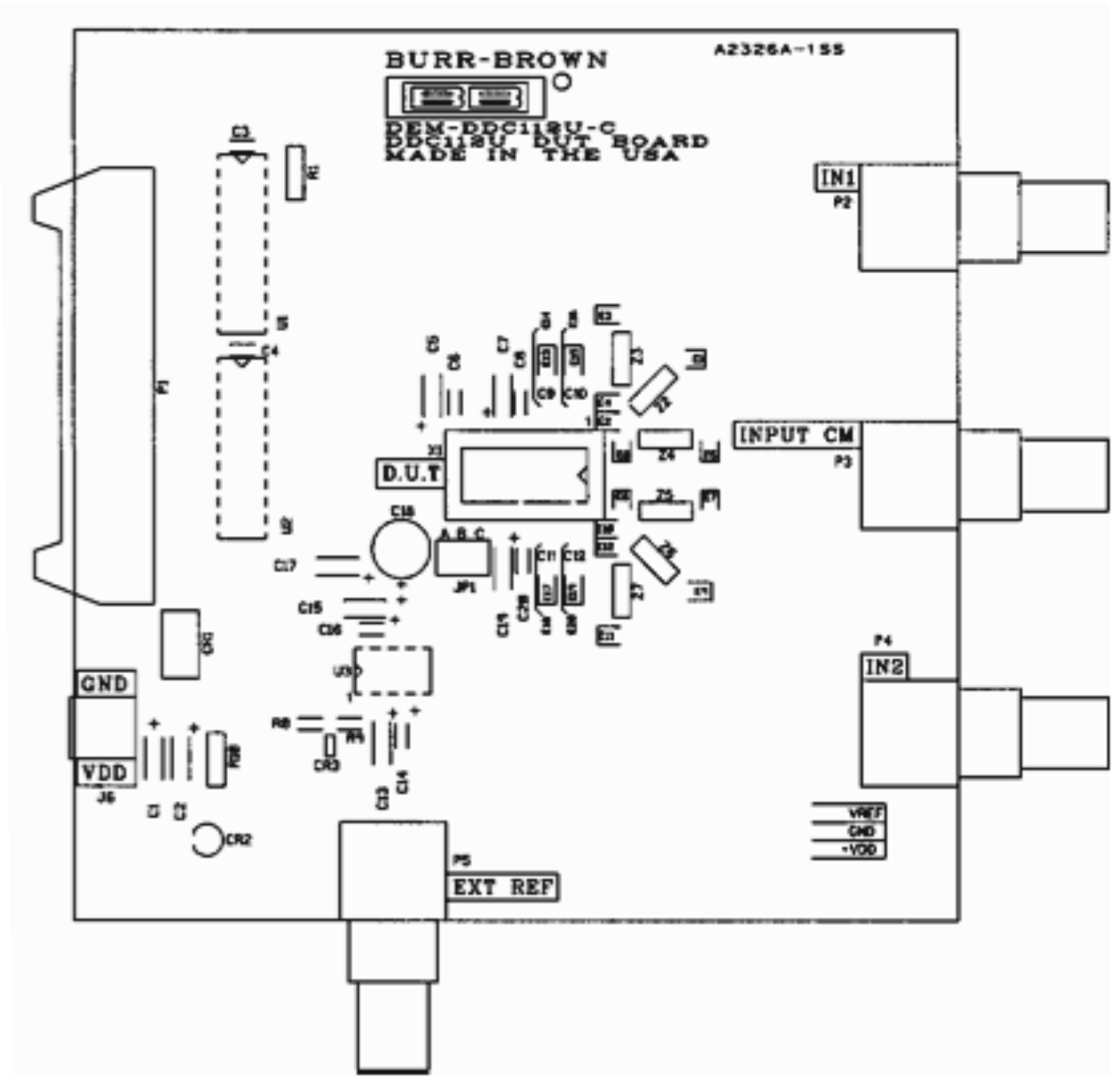


Figure 27. Silkscreen for DEM-DDC112U-C DUT Board

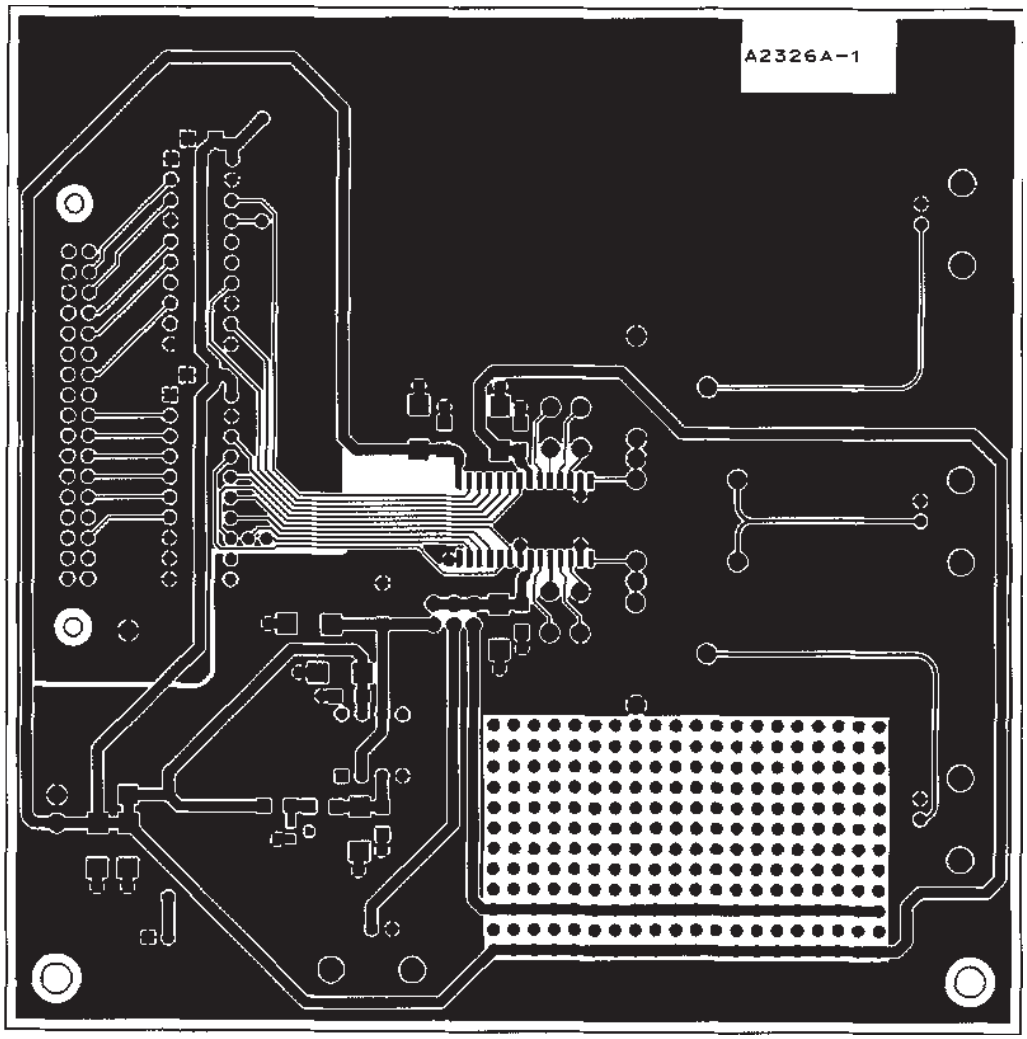


Figure 28. Top Layer of DEM-DDC112U-C DUT Board

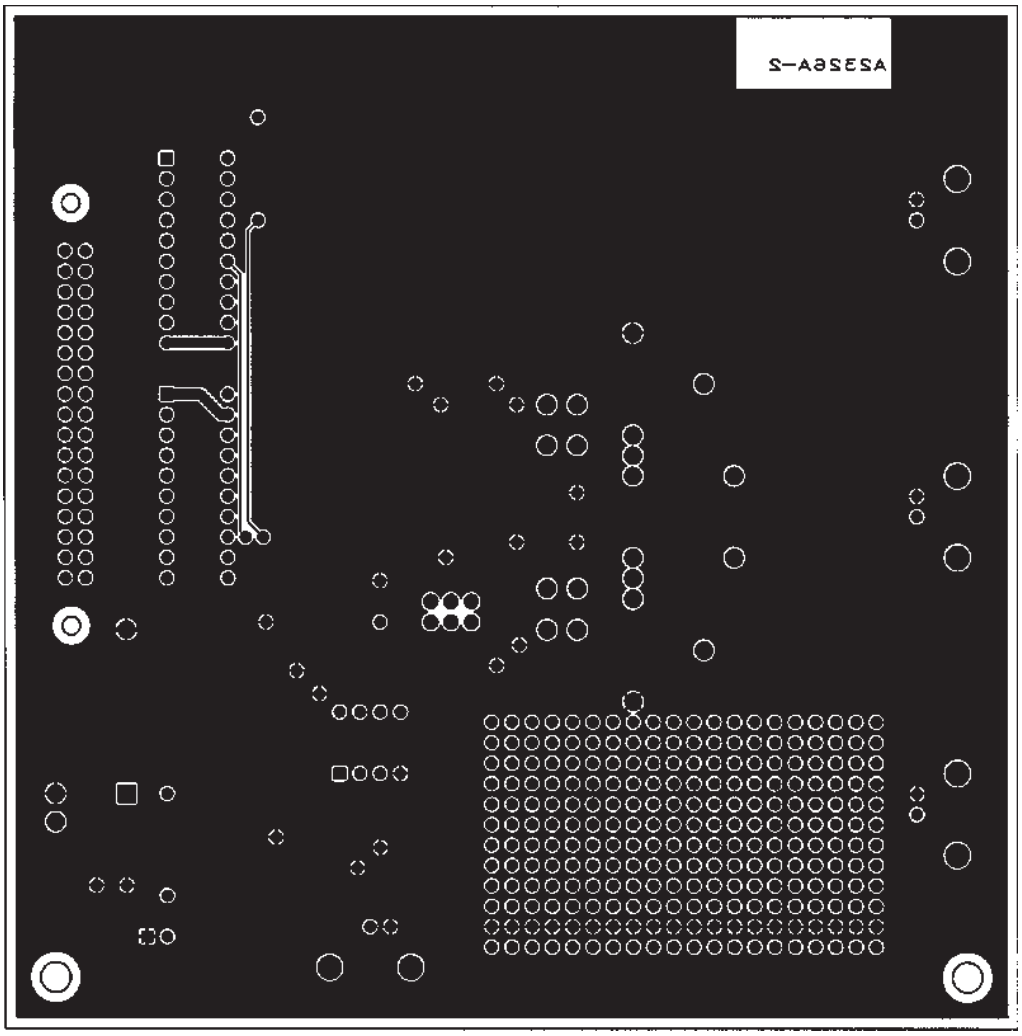


Figure 29. Bottom Layer of DEM-DDC112U-C DUT Board

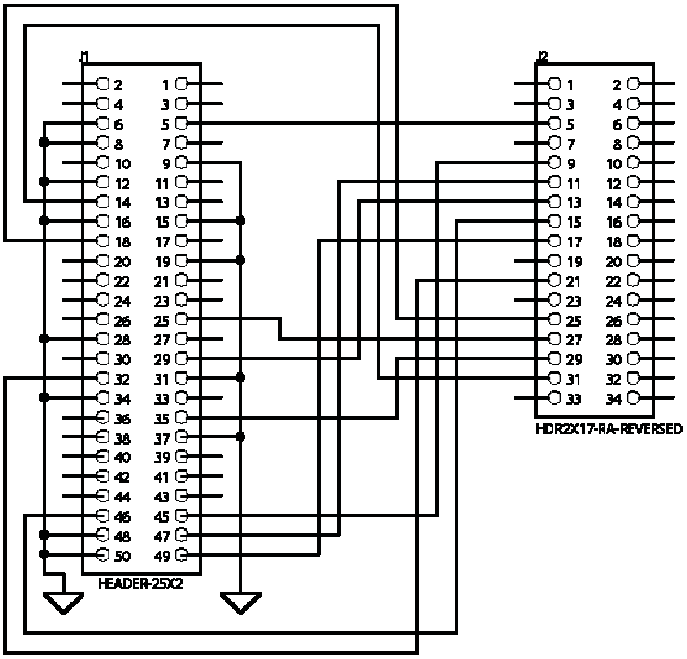


Figure 30. Schematic for DEM-DDC112 Cable Interface Adapter

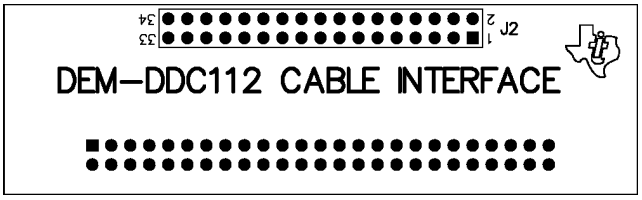


Figure 31. Silkscreen for DEM-DDC112 Cable Interface Adapter

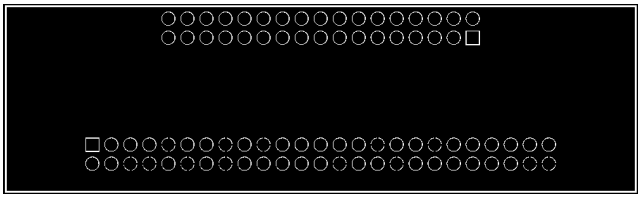


Figure 32. Top Layer of DEM-DDC112 Cable Interface Adapter

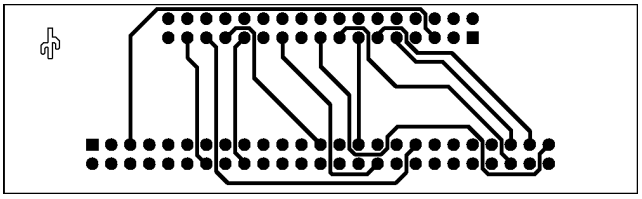


Figure 33. Bottom Layer of DEM-DDC112 Cable Interface Adapter

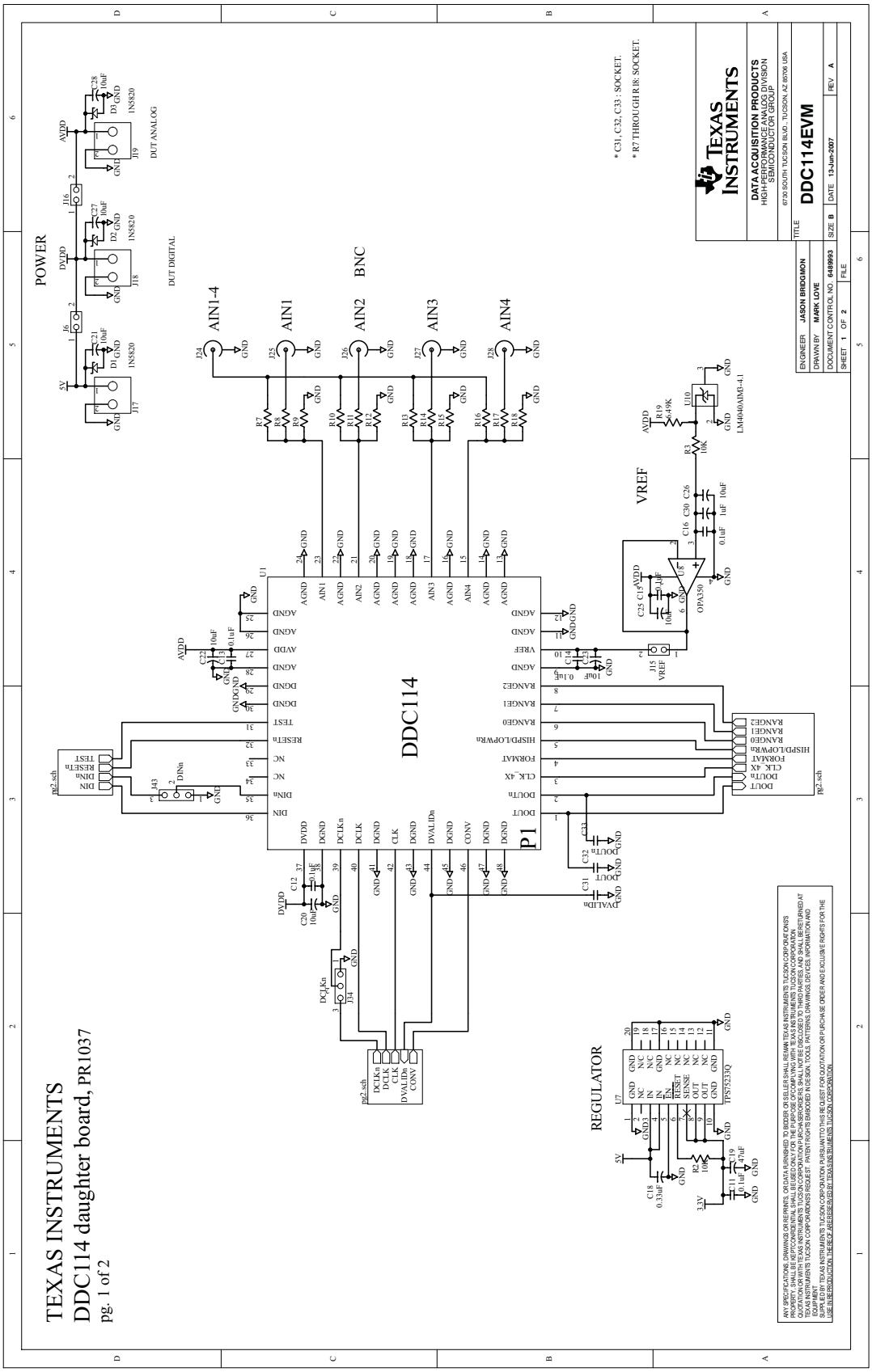


Figure 34. Schematic for DDC114EVM DUT Board (1 of 2)

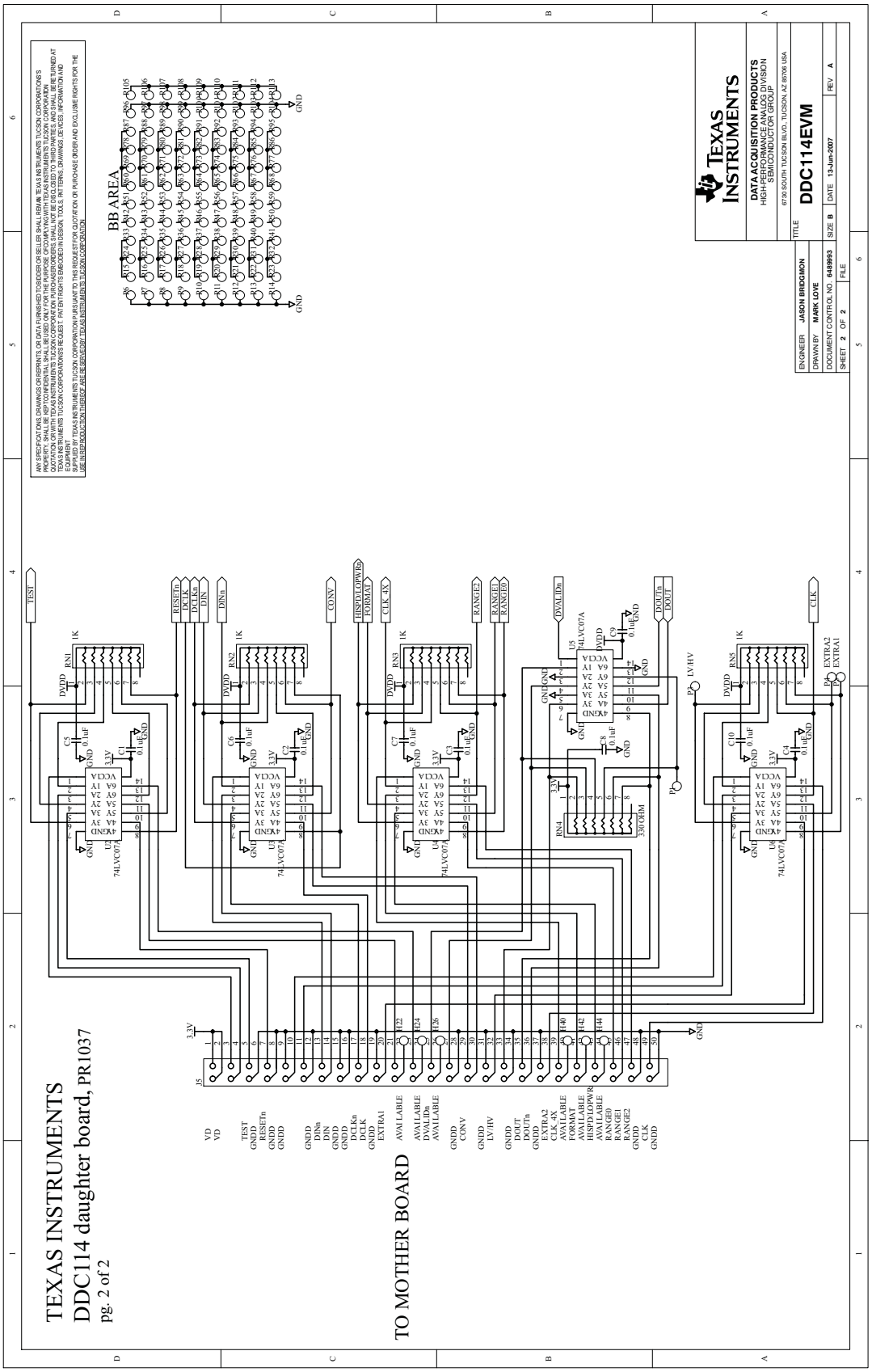


Figure 35. Schematic for DDC114EVM DUT Board (2 of 2)

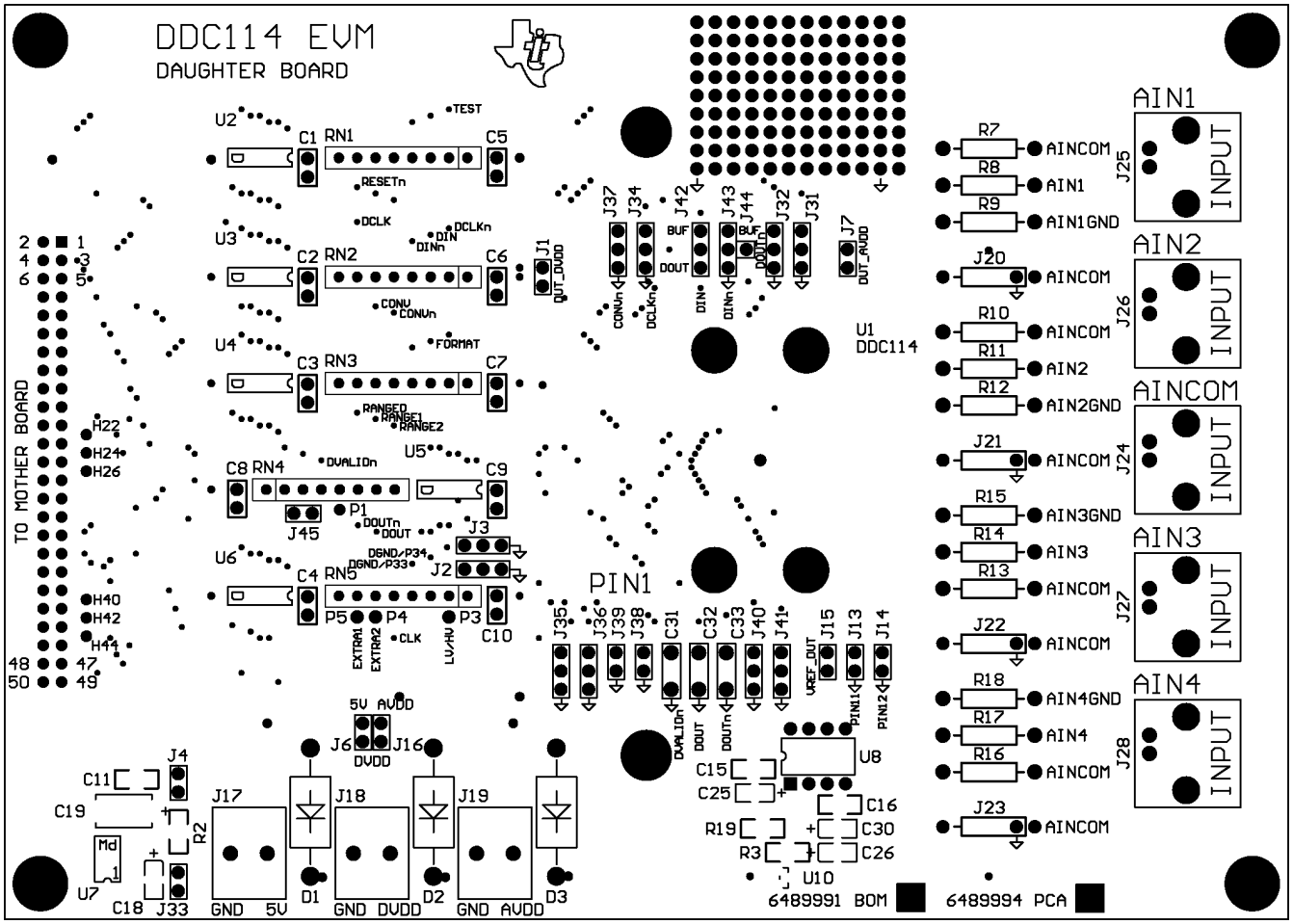


Figure 36. Silkscreen for DDC114EVM DUT Board

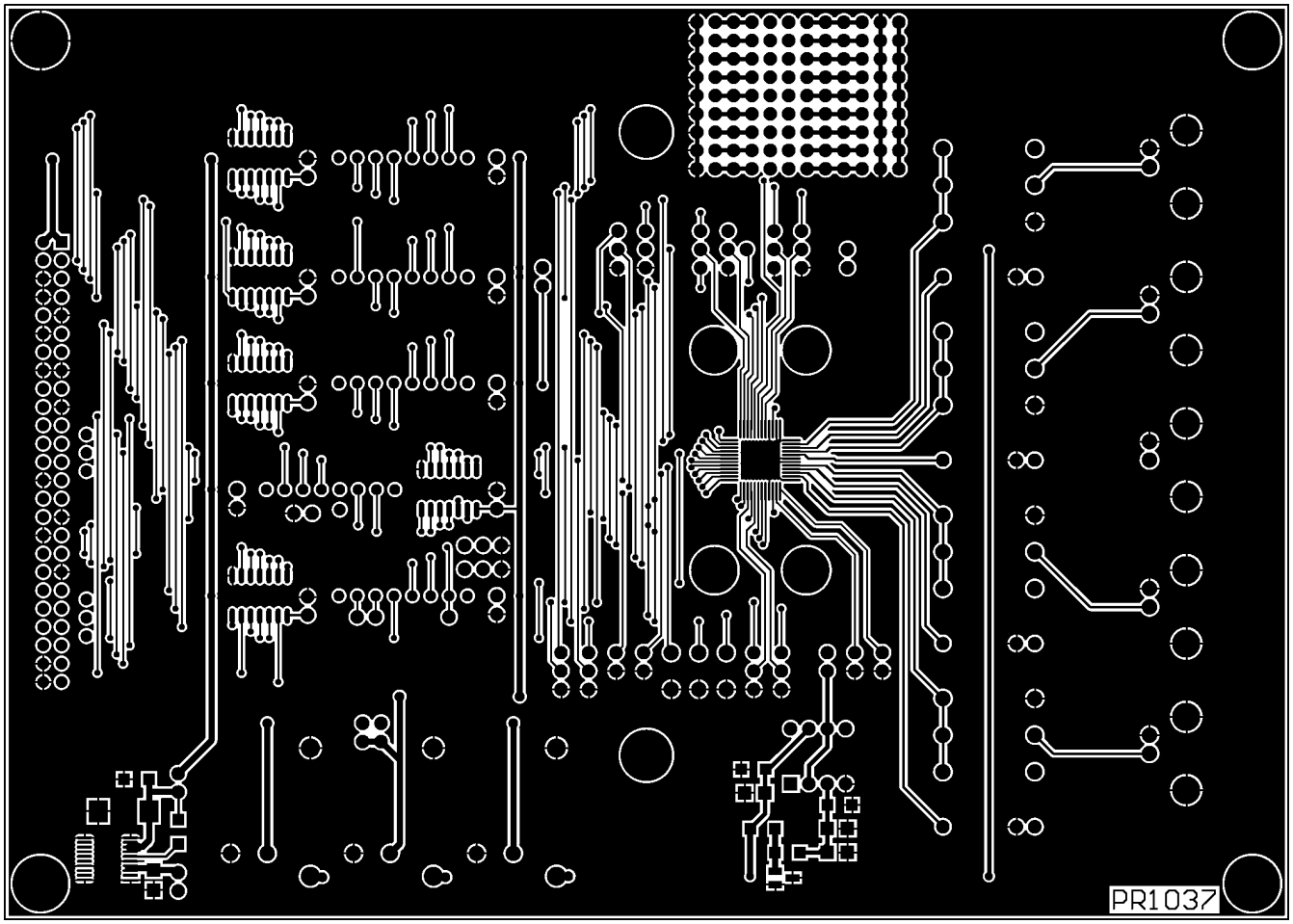


Figure 37. Top Layer of DDC114EVM DUT Board

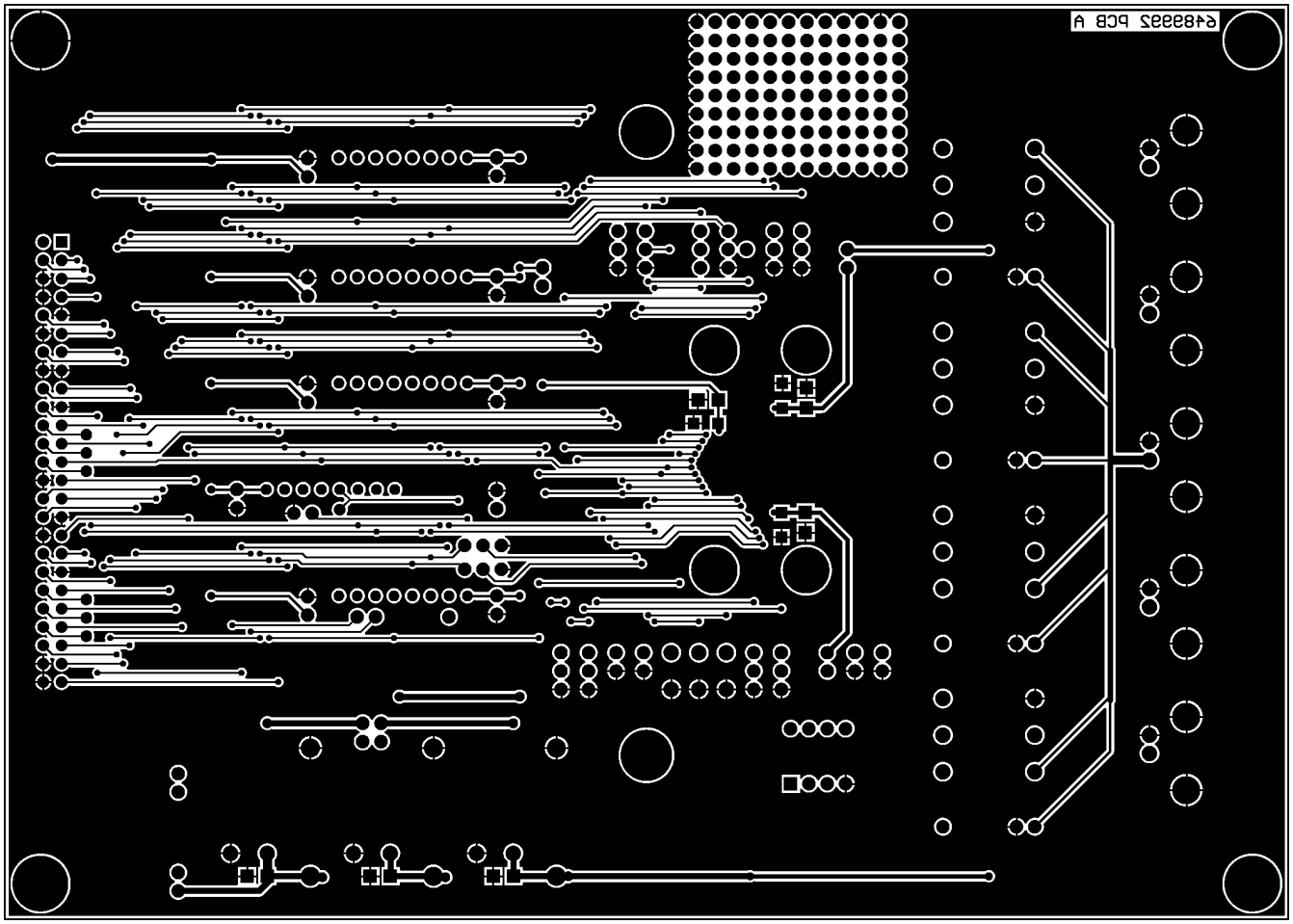


Figure 38. Bottom Layer of DDC114EVM DUT Board

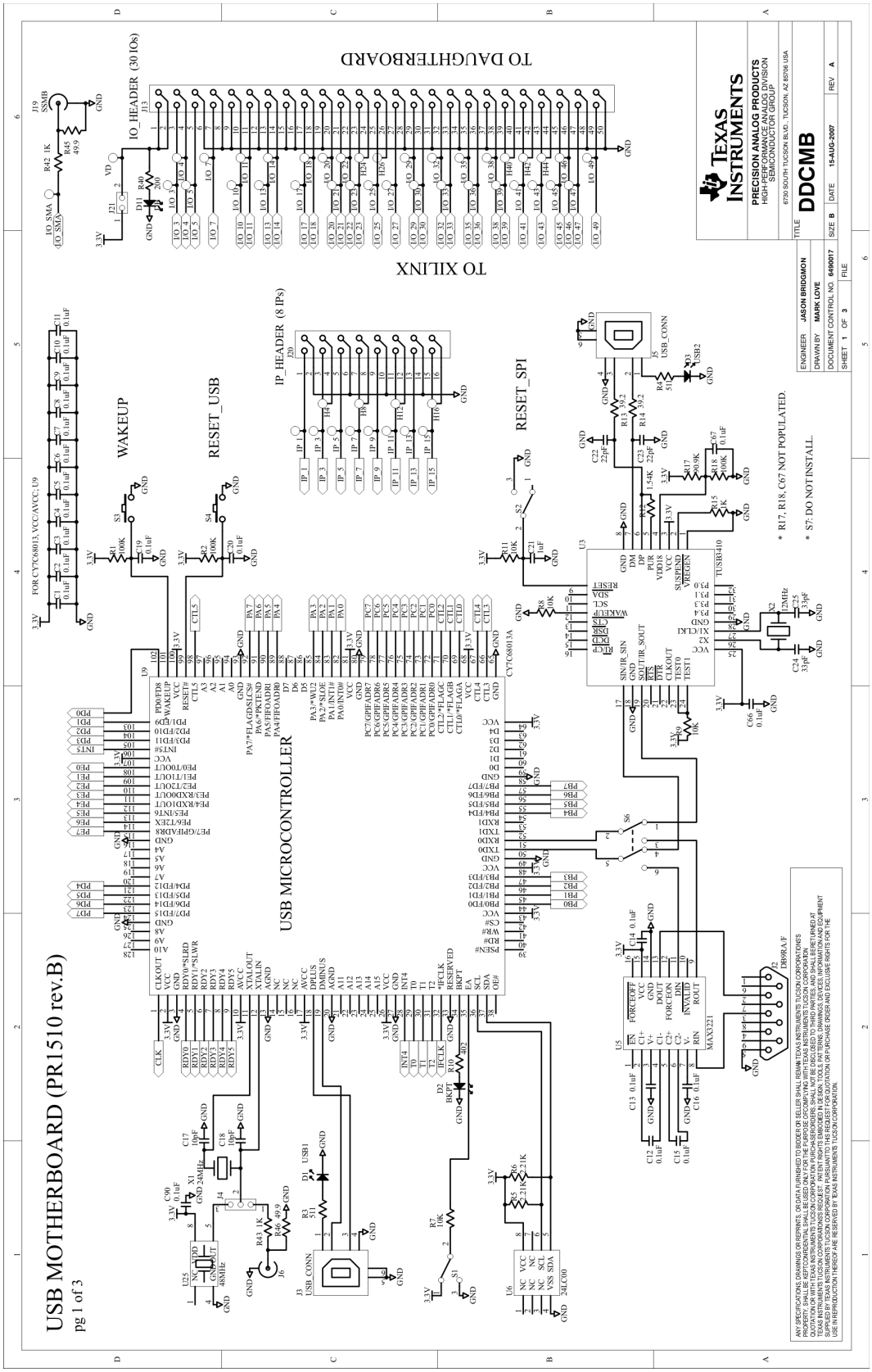


Figure 39. Schematic of DDCMB Motherboard (1 of 3)

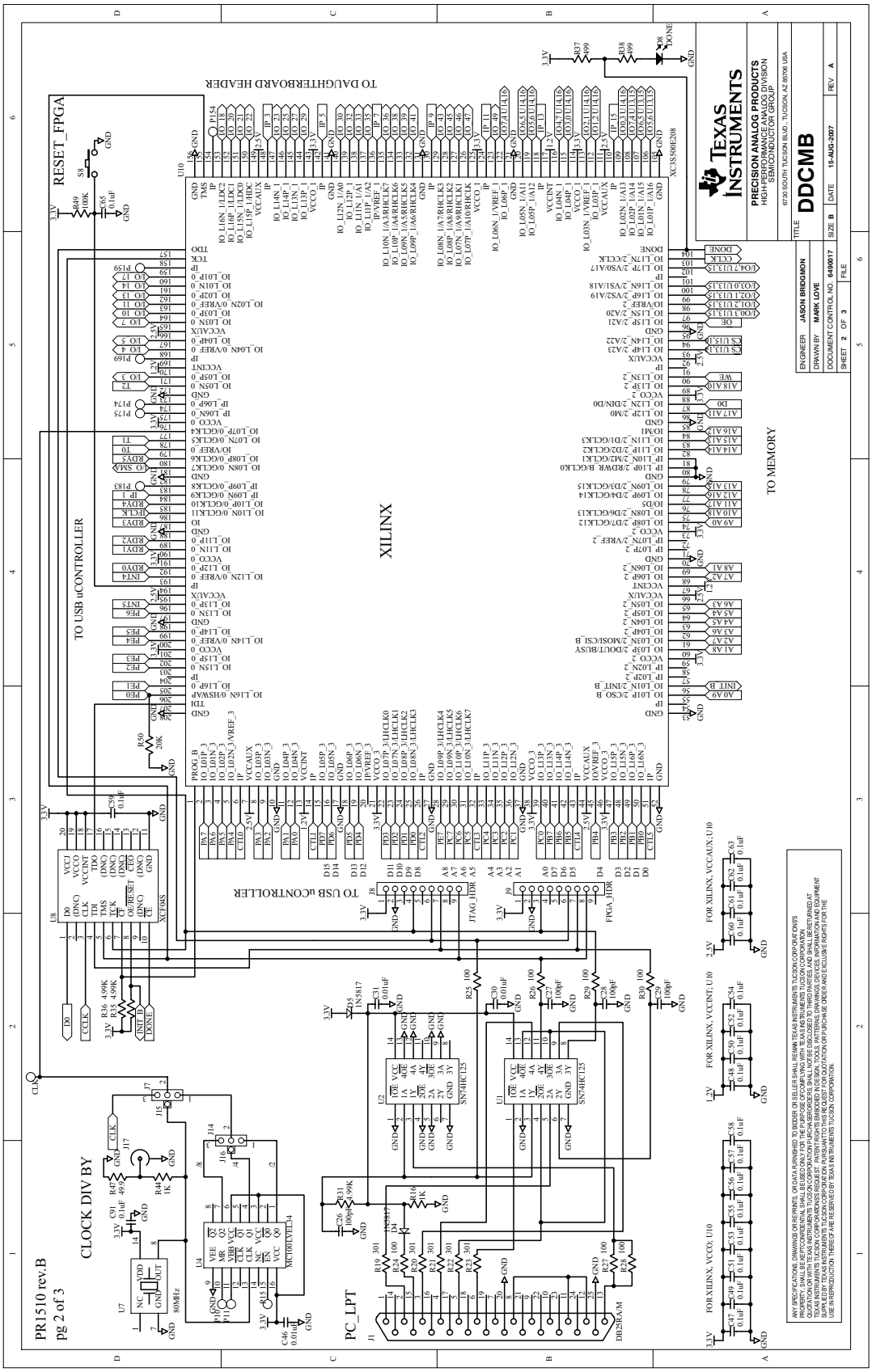


Figure 40. Schematic of DDCMB Motherboard (2 of 3)

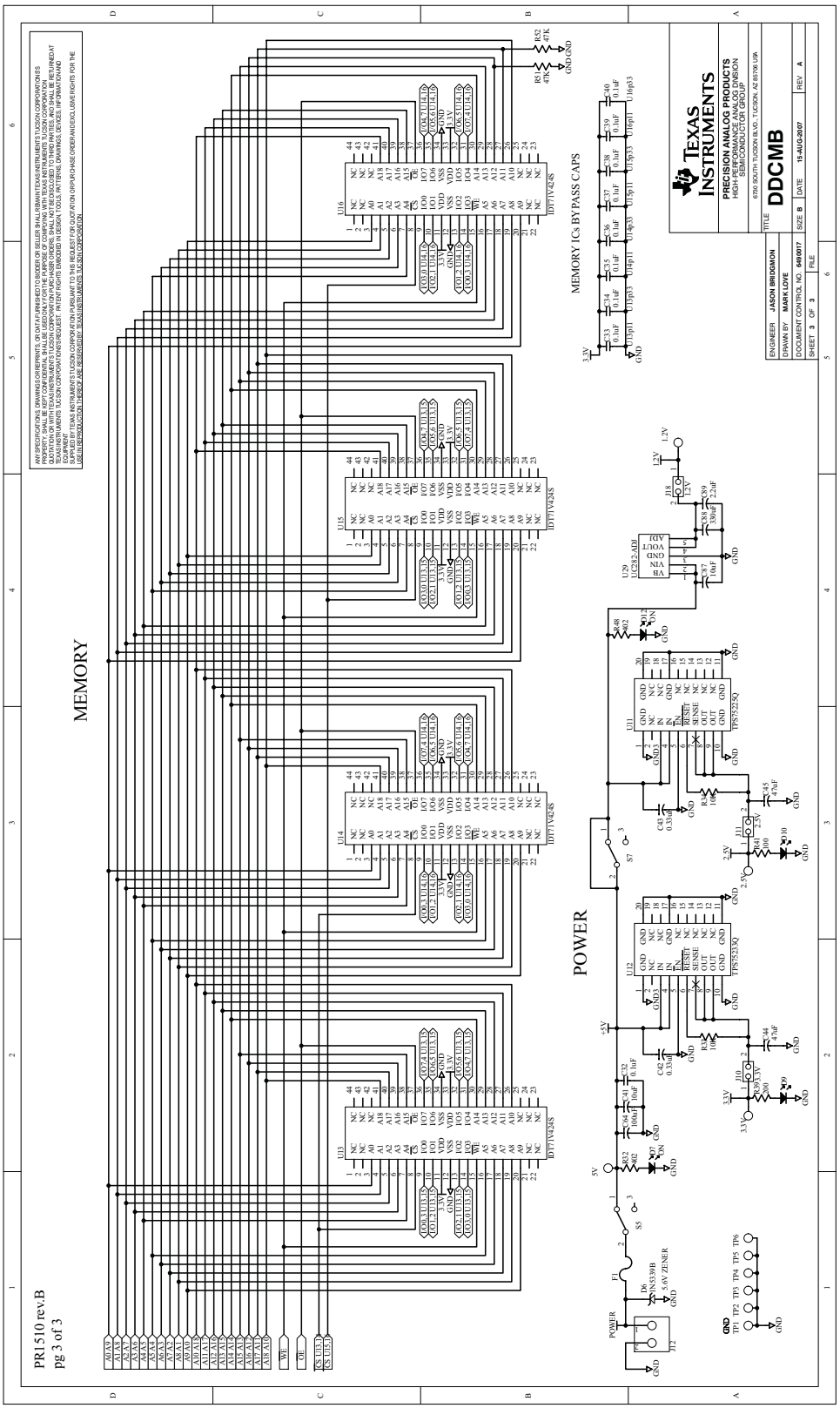


Figure 41. Schematic of DDCMB Motherboard (3 of 3)

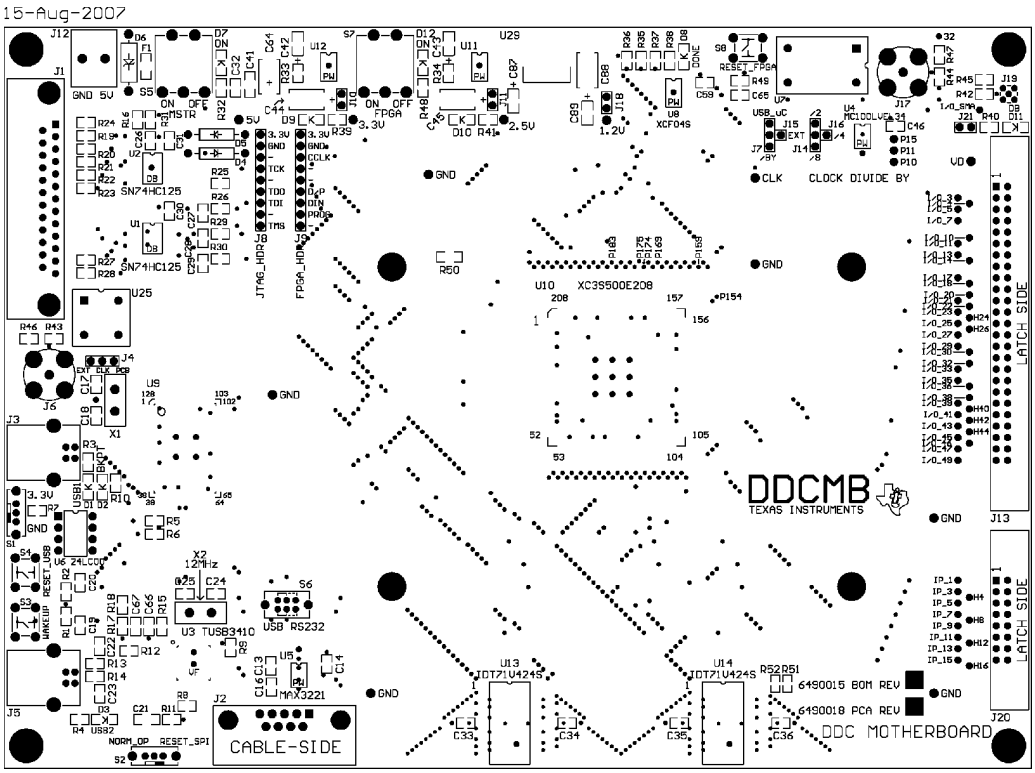


Figure 42. Silkscreen of DDCMB Motherboard

8.1 Bill of Materials

Table 10. DEM-DDC112U-C Bill of Materials

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
1	1	10k	R1	10kΩ, 1%, 1/8W Resistor	Dale	RN55C1002
2	1	4.99k	R8	4.99kΩ, 1%, 1/8W SM Chip Resistor	Dale	CRCW124991F
3	1	10k	R9	10kΩ, 1%, 1/8W SM Chip Resistor	Dale	CRCW12061002F
4	1	1.62k	R10	1.62kΩ, 1%, 1/8W Resistor	Dale	RN55C1621F
Not Installed	4		Z3, Z4, Z5, Z7			
5	2	10M	Z2, Z6	10MΩ, 1%, Resistor	Caddock	MK632, 10M
6	8	10µF	C1, C2, C5, C7, C13, C15, C17, C19	10µF, 20 V, SM Capacitors	Sprague	293D106X9020C2T
7	7	0.1µF	C3, C4, C6, C8, C14, C16, C20	0.1µF SM Capacitors	Kemet	C1206C104K5RAC3972
8	4	270pF	C9, C10, C11, C12	270pF, 100 V, Capacitors	Kemet	C315C271J1G5CA
Not Installed	1		C18			
9	1		U1	Octal Digital Buffer	Texas Instruments	74HCT244N
10	1		U2	Octal Digital Buffer	Texas Instruments	74HCT541N
11	2		U1, U2 (Sockets)	20-pin DIP Socket	Augat	520-AG11D-ES
12	1		X1	Two-Channel A/D Converter	Texas Instruments	DDC112U
13	1		X1 (Socket, Socket Top)	SMT SOP Socket, 0.375 Row Spacing, Body and Frame	Robinson-Nugent	SOP-28B0SMT-TT
14	1		U3	Operational Amplifier	Texas Instruments	OPA350PA
15	1		U3 (Socket)	8-pin DIP Socket	Augat	508-AG11D-ES
16	1		CR3	4.1 Voltage Reference, SOT-23 Package	National Semiconductor	LM4040AIM-4.1
17	1			DDC112 DUT Board	Texas Instruments	A2326
18	1		P4 (Tops)	2-pin Terminal Block Top, 3.5mm Center	RIACON	31165102
19	1		P4 (Pins)	2-pin Terminal Block Pins, 3.5mm Centers	RIACON	31024102
20	1		P1	Right Angle, Connector	Robinson-Nugent	IDH-34LP-SR3-TG
21	4		P2 to P5	Right Angle BNC Connector	AMP	227161-2
22	1		J6 (Pins)	2-pin Terminal Block Pins, 3.5mm Centers	RIACON	31024102

Table 10. DEM-DDC112U-C Bill of Materials (continued)

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
23	1		J6 (Tops)	2-pin Terminal Block Tops, 3.5mm Centers	RIACON	31165102
24	1		CR1	Schottky Diode, 3 A	Motorola	1N5820
25	1		CR2	Red LED	Hewlett-Packard	HLMP-3201
26	20		E1 to E20	Resistor Sockets, Hotlite Socket .0, *E* Point 0.062 Drill	AMP	50863-5
27	1		JP1 (Pins)	Jumper Headers	Samtec	TSW-103-07-T-D
28	1		JP1 (Tops)	Jumper Top (JP1, Position A)	Samtec	SNT-100-BK-T
29	4		Legs	1/4 Inch Hex Spacer, 6-32 Thread	E.F. Johnson	313-6487-008
30	4		To Separate Bottom Ground Plane from DUT Board	1/4 Inch Hex Spacer, 6-32 Thread	E.F. Johnson	313-6487-008
31	2		To Separate Top Ground Plane from DUT Board	3/4 Inch Hinged Spacer, 6-32 Thread	Concord	555-7003-044
32	2		To Separate Top Ground Plane from DUT Board	3/4 Inch Spacer, 6-32 Thread	Concord	542-7612
33	4		To Connect Three Boards	0.75 Inch Round Head Screw, 6-32 Thread		
34	2		To Connect Top	0.25 Inch Round Head Screw, 6-32 Thread		

Table 11. DDC114EVM Bill of Materials

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
1	1	6.49k	R19	1/4W 1% Chip Resistor SMD, 1206	Vishay/Dale	CRCW12066K49FKEA
2	2	10.0k	R2, R3	1/4W 1% Chip Resistor SMD, 1206	Vishay/Dale	CRCW120610K0FKEA
3	1	330	RN4	Bussed Resistor Network, 8-SIP	Bourns Inc.	4608X-101-331LF
4	4	1k	RN1, RN2, RN3,RN5	Bussed Resistor Network, 8-SIP	Bourns Inc.	4608X-101-102LF
5	4	10M	R7, R10, R13, R16	3/4W 1% Radial Film Resistor	Caddock	MK632-10.0M-1%
6	6	0.1µF	C11 to C16	100V Ceramic Chip Capacitor, ±10%, X7R, 1206	TDK	C3216X7R2A104K
7	10	0.1µF	C1 to C10	50V Ceramic Radial Capacitor, ±10%	Kemet	C320C104K5R5TA
8	1	0.33µF	C18	35V Tantalum Chip Capacitor, ±10%, SMD, 3216	Kemet	T491A334K035AT
9	1	1µF	C30	16V Tantalum Chip Capacitor, ±10%, SMD, 3216	Kemet	T491A105K016AT
10	8	10µF	C20 to C23, C25 to C28	10V Tantalum Chip Capacitor, ±10%, SMD, 3216	Kemet	T491A106K010AT
11	1	47µF	C19	16V Tantalum Chip Capacitor, ±10%, SMD, 7343	Kemet	T491D476K016AT
12	1		U1	20-bit Quad Input ADC, 48-QFN	Texas Instruments	DDC114IRTCT
13	5		U2-U6	Hex Buffer/Driver w/Open Drain	Texas Instruments	SN74LVC07AD
14	1		U7	3.3 V, 2 A LDO Regulator 20-HTSSOP	Texas Instruments	TPS75233QPWP
15	1		U8	CMOS Op Amp 8-DIP	Texas Instruments	OPA350PA
16	1		U10	Precision Reference	National Semiconductor	LM4040AIM3-4.1
17	2		J6, J16	1 X 2 Header	Samtec	TSW-102-07-G-S
18	3		J17, J18, J19	Terminal Block, 5mm, 2 Position	On Shore Technology	ED300/2
19	5		J24-J28	Connector BNC R/A 50 Ω Tin	Tyco/AMP	227161-2
20	1		J5	Connector Header R/A 50 Position, .100, 15AU	Tyco/AMP	1-5102162-0
Not Installed	3		J2, J3, J44			
21	1		N/A	DDC114VM PWB	Texas Instruments	6489992

Table 11. DDC114EVM Bill of Materials (continued)

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
22	2		N/A	DDC114EVM-Shield PWB	Texas Instruments	6489997
23	3		D1, D2, D3	20V, 3A, Schottky Diode	ON Semiconductor	1N5820RLG
24	30		C31 to C33, R7 to R18	Connector Socket Receptacle	Tyco/AMP	5050863-5
25	20		J1, J4, J7, J13 to J15, J31 to J43, J45	Buss Wire 22 AWG, Solid		
26	4		J20, J21, J22, J23	Insulated Wire 22 AWG, Solid		
27	2		N/A	Lock Ejector Hooks for J15	Tyco/AMP	102320-1
28	8		N/A	Machine Screws, Phillips Head 4-40 x 1/45	Building Fasteners	PMSSS 440 0025 PH
29	4		N/A	Hex Standoff M/F 4-40, .500, Aluminum	Keystone Electronics	8401
30	2		N/A	Hex Standoff 4-40 Through, .750, Aluminum	Keystone Electronics	2204
31	2		N/A	Hex Standoff F/F Hinged 4-40	Keystone Electronics	351
32	2		N/A	Hex Standoff 4-40 Through, .500, Aluminum	Keystone Electronics	2203
33	1		N/A	Shorting Block	Samtec	SNT-100-BK-G-H

Table 12. DDCMB Bill of Materials

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
1	2	49.9	R45, R47	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF49R9V
2	8	100	R24 to R30, R41	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF1000V
3	2	200	R39, R40	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF2000V
4	5	301	R19 to R23	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF3010V
5	3	402	R10, R32, R48	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF4020V
6	2	499	R37, R38	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF4990V
7	1	511	R3	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF5110V
8	3	1k	R16, R42, R44	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF1001V
9	2	2.21k	R5, R6	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF2211V
10	3	4.99k	R31, R35, R36	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF4991V
11	3	10k	R7, R33, R34	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF1002V
12	1	20k	R50	1/4W 1% Chip Resistor SMD, 1206	Panasonic	ERJ-8ENF2002V
13	2	47.5k	R51, R52	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF4752V
14	3	100k	R1, R2, R49	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF1003V
Not Installed	2	39.2	R13, R14	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF39R2V
Not Installed	1	49.9	R46	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF49R9V
Not Installed	1	511	R4	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF5110V
Not Installed	2	1k	R15, R43	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF1001V
Not Installed	1	1.54k	R12	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF1541V

Table 12. DDCMB Bill of Materials (continued)

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
Not Installed	3	10k	R8, R9, R11	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF1002V
Not Installed	1	90.9k	R17	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF9092V
Not Installed	1	100k	R18	1/8W 1% Chip Resistor SMD, 0805	Panasonic	ERJ-6ENF1003V
15	2	10pF	C17, C18	100V Ceramic Chip Capacitor, ±5%, C0G, 0805	Murata	GRM2195C2A100JZ01D
16	1	100pF	C26	100V Ceramic Chip Capacitor, ±5%, C0G, 0805	Murata	GRM2165C2A101JA01D
17	3	0.01µF	C30, C31, C46	100V Ceramic Chip Capacitor, ±10%, X7R, 0805	TDK	C2012X7R2A103K
18	41	0.1µF	C1 to C11, C19 to C20, C32 to C40, C47 to C63, C65, C91	100V Ceramic Chip Capacitor, ± 10%, X7R, 0805	TDK	C2012X7R2A104K
19	2	0.33µF	C42, C43	35V Tantalum Chip Capacitor, ±10%, SMD, 3216	Kemet	T491A334K035AT
20	1	2.2µF	C89	16V Tantalum Chip Capacitor, ±10%, SMD, 3216	Kemet	T491A225K016AT
21	1	10µF	C41	16V Ceramic Chip Capacitor, ±20%, X7R, 1206	TDK	C3216X7R1C106M
22	1	10µF	C87	10V Tantalum Chip Capacitor, ±10%, SMD, 3216	Kemet	T491A106K010AT
23	2	47µF	C44, C45	16V Tantalum Chip Capacitor, ±10%, SMD, 7343	Kemet	T491D476K016AT
24	1	100µF	C64	16V Tantalum Chip Capacitor, ±10%, SMD, 7343	Kemet	T491D107K016AT
25	1	330µF	C88	10V Tantalum Chip Capacitor, ±20%, SMD, 7343	Kemet	T491D337M010AT
Not Installed	2	22pF	C22, C23	100V Ceramic Chip Capacitor, ±5%, C0G, 0805	Murata	GRM2195C2A220JZ01D
Not Installed	2	33pF	C24, C25	100V Ceramic Chip Capacitor, ±5%, C0G, 0805	Murata	GRM2195C2A330JZ01D
Not Installed	3	100pF	C27, C28, C29	100V Ceramic Chip Capacitor, ±5%, C0G, 0805	Murata	GRM2165C2A101JA01D

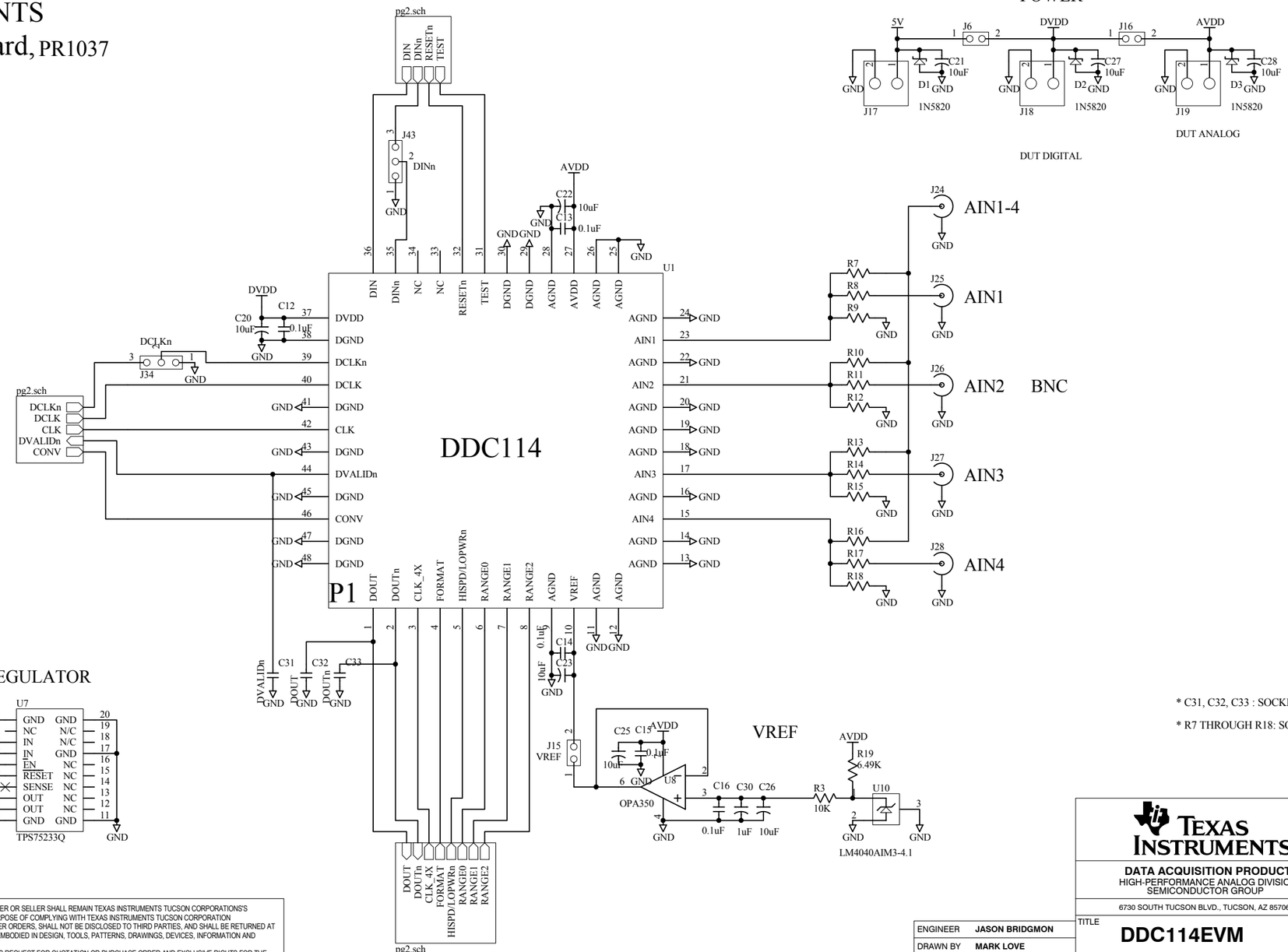
Table 12. DDCMB Bill of Materials (continued)

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
Not Installed	8	0.1µF	C12-C16, C66-C67, C90	100V Ceramic Chip Capacitor, ±10%, X7R, 0805	TDK	C2012X7R2A104K
Not Installed	1	1µF	C21	50V Ceramic Chip Capacitor, ±10%, X7R, 1206	TDK	C3216X7R1H105K
26	1		U6	5V, Serial EEPROM 128 bit, DIP	Microchip	24LC00-I/P
27	1		U9	USB Hi-Speed Peripheral IC	Cypress	CY7C68013A-128AXC
28	1	80.0	U7	3.3V Oscillator, ±50ppm	ECS Inc.	ECS-UPO-14PINX
29	4		U13, U14, U15, U16	4MB SRAM IC	IDT	IDT71V424S10PHG
				alternate	IDT	IDT71V424S10PHIG
30	2		U1, U2	Quad Bus Buffer, Tri-State	Texas Instruments	SN74HC125DBR
31	1		U11	2.5V, 2A LDO Regulator	Texas Instruments	TPS75225QPWP
32	1		U12	3.3V, 2A LDO Regulator	Texas Instruments	TPS75233QPWP
33	1		U29	1.2V/Adj. Fast LDO Regulator	Texas Instruments	UC282TDKTTT-ADJ
34	1		U10	FPGA, 10476 Logic Cells	Xilinx	XC3S500E-4PQG208C
35	1		U8	3.3V PROM	Xilinx	XCF04SVOG20C
Not Installed	1	48.0	U25	3.3V Oscillator, ±30ppm	Abracon	ACHL-48.000MHZ-EK
Not Installed	1		U3	USB to Serial Converter	Texas Instruments	TUSB3410VF
Not Installed	1		U5	RS-232 Line Driver/Receiver	Texas Instruments	MAX3221CPWR
Not Installed	1		U4	Clock Generator IC	ON Semiconductor	MC100LVEL34DTG
36	1		J1	Connector D-Sub, 25 Pos, RA	Tyco/AMP	5747842-4
37	1		J3	Connector, USB Type B, PCB	Mill-Max	897-43-004-90-000000
38	1		J12	Terminal Block, 5mm, 2 Position	On Shore Technology	ED300/2
39	1		J13	Connector Header, .1, 50 Position, RA	Tyco/AMP	1-5102162-0
40	1		J17	Connector BNC, 50 Ω, Vertical	Tyco/AMP	5414305-1
41	1		J15	1 X 1 Header	Samtec	TSW-101-07-G-S
42	2		J11, J21	1 X 2 Header	Samtec	TSW-102-07-G-S
43	1		J7	1 X 3 Header	Samtec	TSW-103-07-G-S
44	2		J8, J9	1 X 9 Header	Samtec	TSW-109-07-G-S
Not Installed	1		J5	Connector, USB Type B, PCB	Mill-Max	897-43-004-90-000000
Not Installed	1		J6	Connector BNC, 50 Ω, Vertical	Tyco/AMP	5414305-1

Table 12. DDCMB Bill of Materials (continued)

Item No.	Qty	Value	Ref Designator	Description	Vendor	Part Number
Not Installed	1		J20	Shrouded Header, .1, 16 Position, RA	Tyco/AMP	5102322-3
Not Installed	1		J2	Connector D-Sub Receptacle R/A 9 Position	Tyco/AMP	5747844-2
Not Installed	1		J19	SSMB Jack, PCB	Pasternack Enterprises	PE4340
Not Installed	1		J16	1 X 1 Header	Samtec	TSW-101-07-G-S
Not Installed	2		J4, J14	1 X 3 Header	Samtec	TSW-103-07-G-S
45	1		N/A	DDCMB PWB	Texas Instruments	6490016
46	3		D1, D2, D11	LED Green, SMD 1206	Lumex	SML-LX1206GC-TR
47	5		D7, D8, D9, D10, D12	LED Red, SMD 1206	Lumex	SML-LX1206IC-TR
48	2		D4, D5	20V, 1A, Schottky Diode	Diodes Inc.	1N5817-T
49	1		D6	5.6V Zener Diode	ON Semiconductor	1N5339BRLG
Not Installed	1		D3	LED Green, SMD 1206	Lumex	SML-LX1206GC-TR
50	1		F1	63V, 2A Fast Fuse, SMD, 1206	Tyco, Raychem Circuit Protection	1206SFF200F/63-2
51	2		J10, J18	Buss Wire 22 AWG, Solid		
52	1		S1	SPDT Slide Switch, RA	E-Switch	EG1213
53	3		S3, S4, S8	Momentary Tactile Switch, 6mm, 100gf	Omron Electronics Inc.	B3F-1050
54	1		S5	SPDT Toggle Switch, RA	ITT/C&K	7101MD9AGE
Not Installed	1		S2	SPDT Slide Switch, RA	E-Switch	EG1213
Not Installed	1		S6	DPDT Slide Switch	E-Switch	EG2207
Not Installed	1		S7	SPDT Toggle Switch, RA	ITT/C&K	7101MD9AGE
55	1	24.000	X1	Crystal, 16pF, HC49/US	ECS Inc.	ECS-240-16-4X
Not Installed	1	12.000	X2	Crystal, 16pF, HC49/US	ECS Inc.	ECS-120-16-4X
56	2		N/A	Lock Ejector Hooks for J13	Tyco/AMP	102320-1
56	8		N/A	Machine Screws, Phillips Head 6-32 x 5/16	Building Fasteners	PMSSS 632 0031 PH
56	8		N/A	Hex Standoff 6-32, .625	Keystone Electronics	1813
57	2		N/A	Shorting Block	Samtec	SNT-100-BK-G-H

TEXAS INSTRUMENTS
DDC114 daughter board, PR1037
pg. 1 of 2



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SEMICONDUCTOR GROUP
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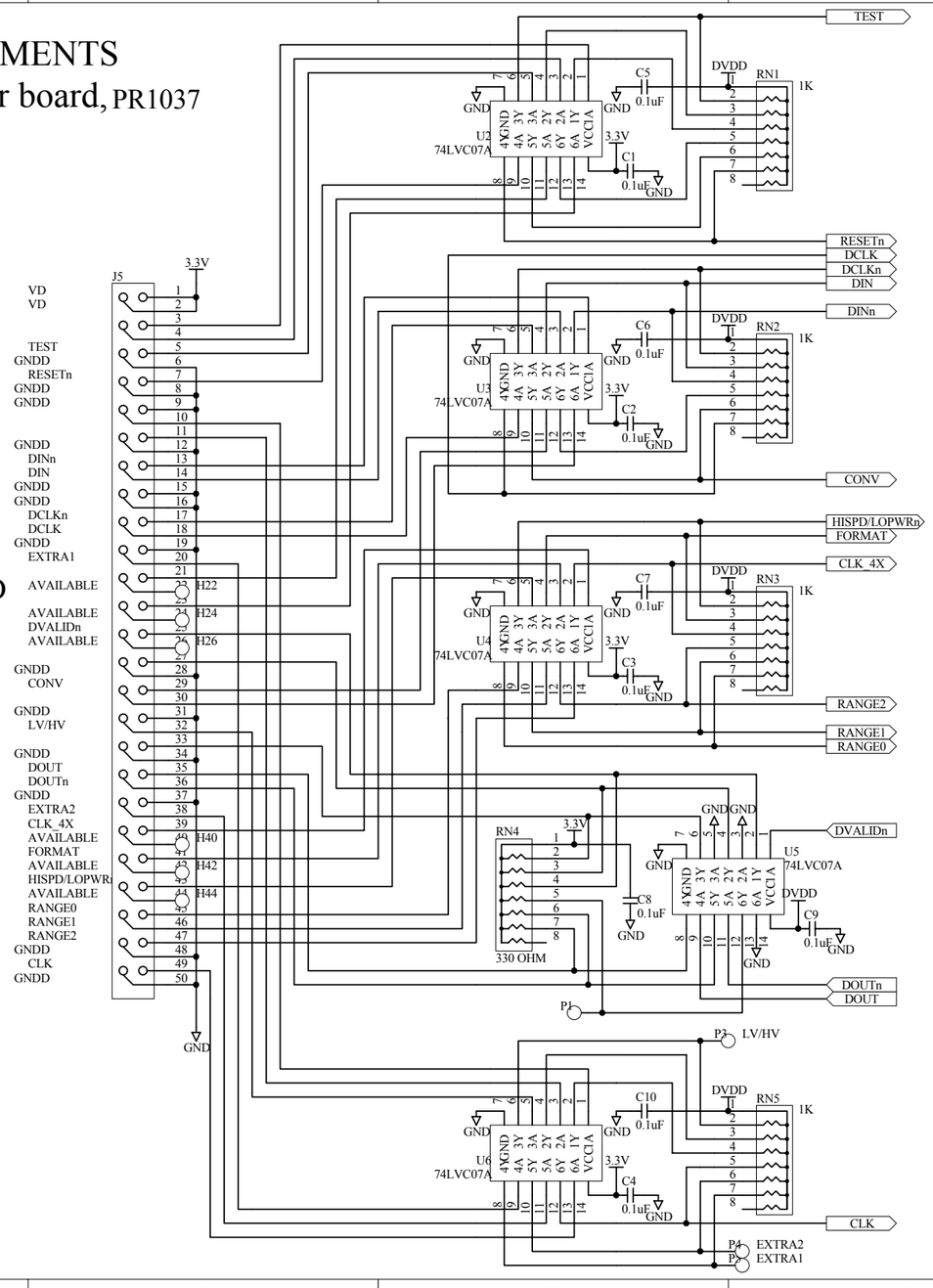
ENGINEER **JASON BRIDGMON**	TITLE **DDC114EVM**		
DRAWN BY **MARK LOVE**			
DOCUMENT CONTROL NO. **6489993**	SIZE **B**	DATE **13-Jun-2007**	REV **A**
SHEET **1** OF **2**	FILE		

TEXAS INSTRUMENTS
DDC114 daughter board, PR1037
pg. 2 of 2

TO MOTHER BOARD



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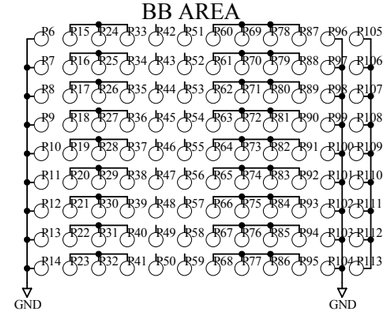

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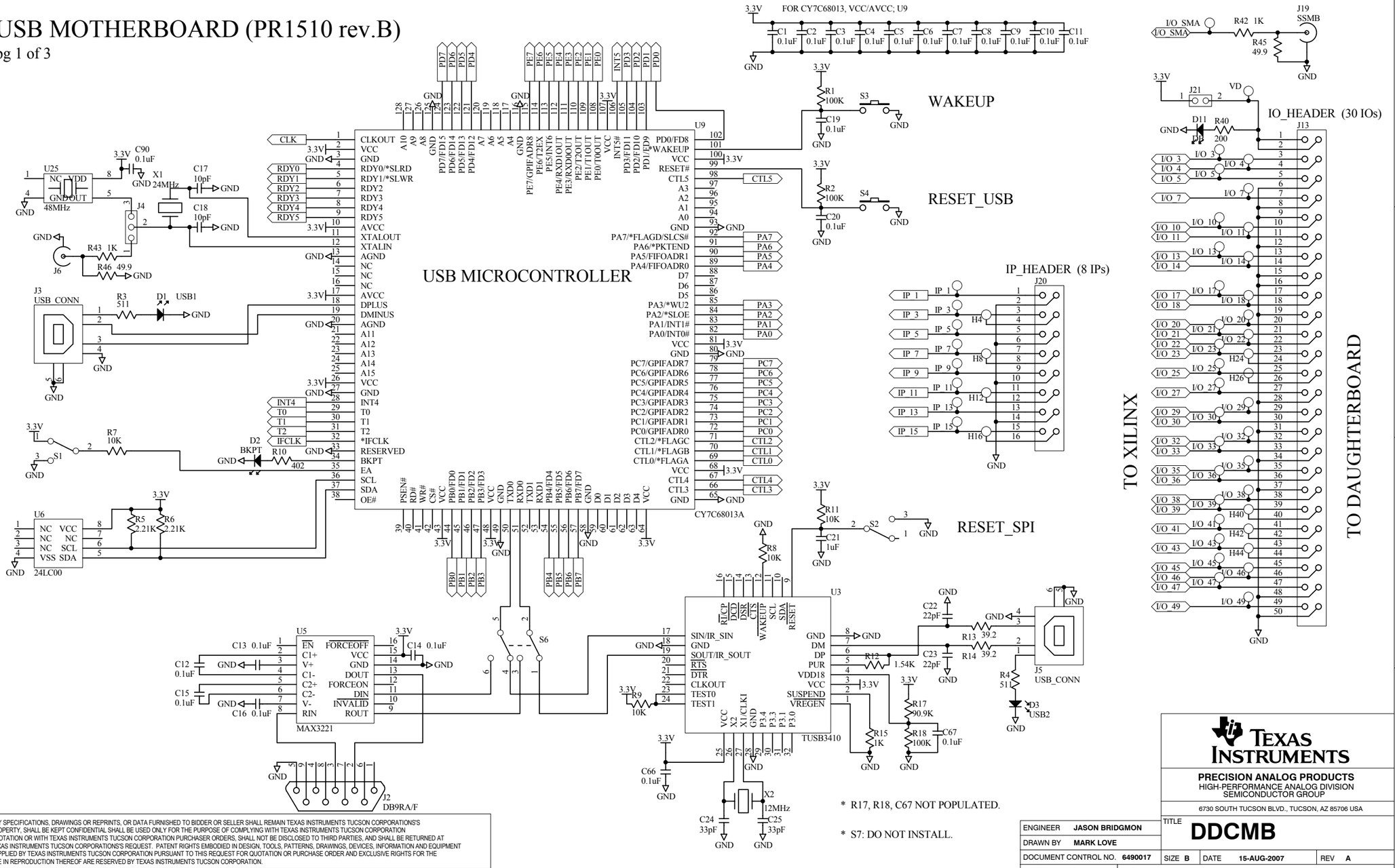
SHEET **2** OF **2**	FILE		

USB MOTHERBOARD (PR1510 rev.B)

pg 1 of 3



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ENGINEER **JASON BRIDGMON**	TITLE **DDCMB**		
DRAWN BY **MARK LOVE**			
DOCUMENT CONTROL NO. **6490017**	SIZE **B**	DATE **15-AUG-2007**	REV **A**
SHEET **1** OF **3**	FILE		

PR1510 rev.B
pg 2 of 3

CLOCK DIV BY

U7 80MHz — C91 0.1uF — R47 49.9 — R44 1K — J17 — J15 — J7

U4 MC100LVEL34 — /8 — /4 — /2 — J14 — J16 — C46 0.01uF — R15

PC_LPT

J1 DB25RA/M — D4 1N5817 — C26 100pF — R31 4.99K — R16 1K — R19 301 — R24 100 — R20 301 — R21 301 — R22 301 — R23 301 — R27 100 — R28 100

U2 SN74HC125 — C31 0.01uF

U1 SN74HC125 — C30 0.01uF — C27 100pF — C28 100pF — C29 100pF — R25 100 — R26 100 — R29 100 — R30 100

D5 1N5817

J8 JTAG_HDR — J9 FPGA_HDR

R36 4.99K — R35 4.99K

U8 XCF04S — C59 0.1uF

D0 — CCLK — INIT_B — DONE

CLK

R50 20K

TO USB uCONTROLLER

TO USB uCONTROLLER

XILINX

RESET_FPGA — R49 100K — S8 — C65 0.1uF

TO DAUGHTERBOARD HEADER

U10 XC3S500E208

R37 499 — R38 499 — D8 DONE

TO MEMORY

FOR XILINX, VCCO; U10 — C47 C49 C51 C53 C55 C56 C57 C58 0.1uF

FOR XILINX, VCCINT; U10 — C48 C50 C52 C54 0.1uF

FOR XILINX, VCCAUX; U10 — C60 C61 C62 C63 0.1uF

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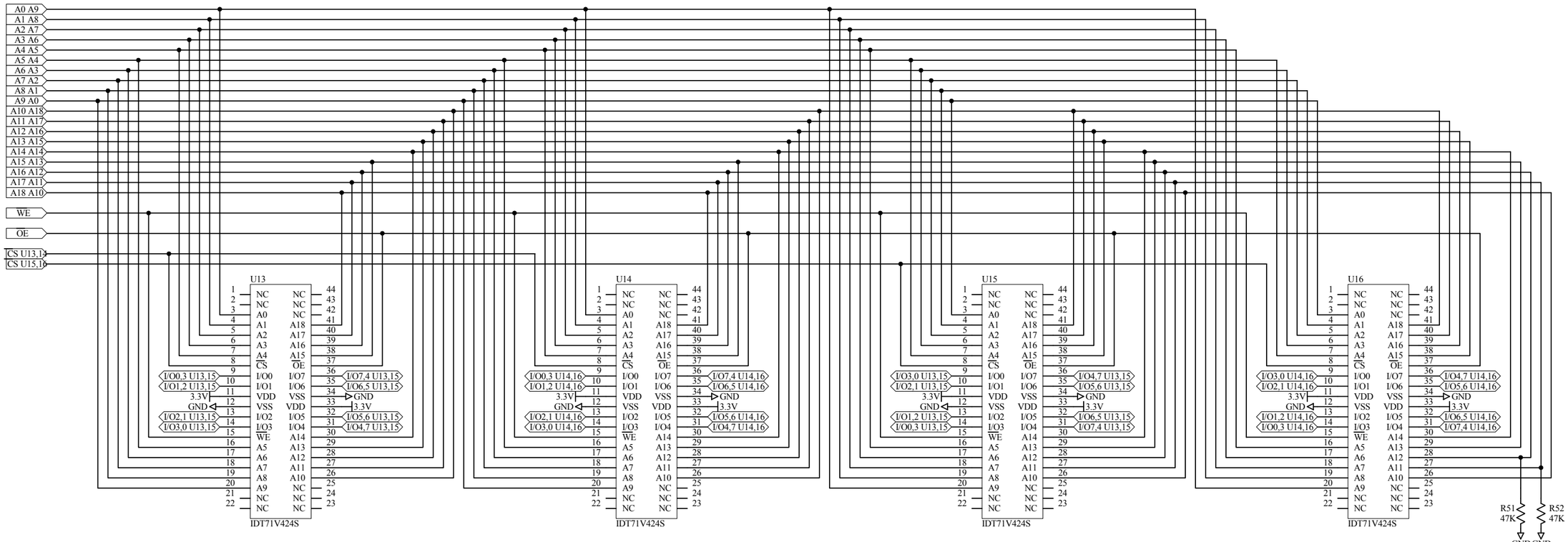
ENGINEER JASON BRIDGMON	TITLE DDCMB		
DRAWN BY MARK LOVE			
DOCUMENT CONTROL NO. 6490017	SIZE B	DATE 15-AUG-2007	REV A
SHEET 2 OF 3	FILE		

PR1510 rev.B
pg 3 of 3

MEMORY



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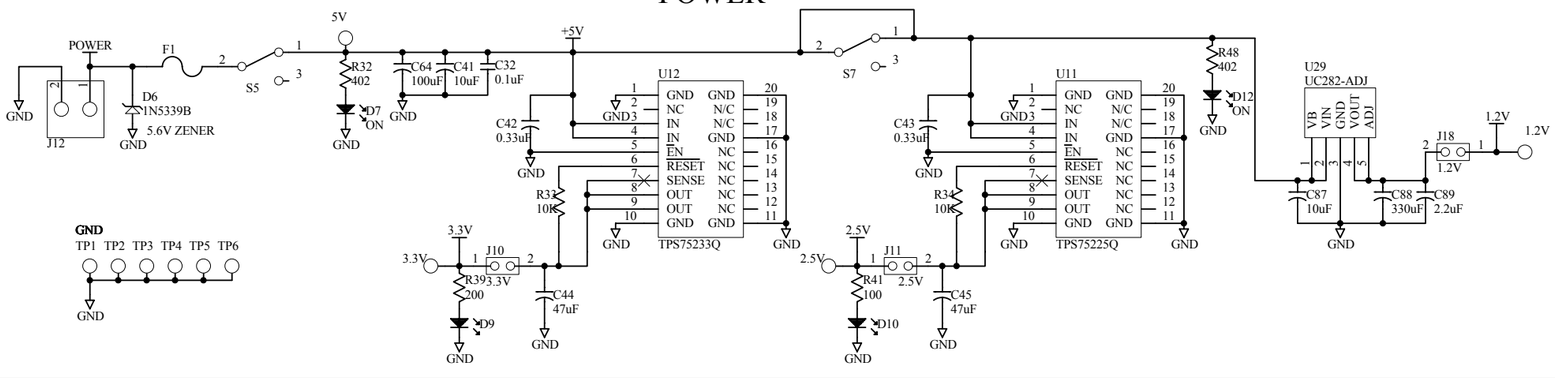
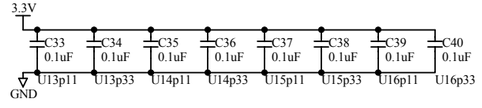


MEMORY ICs BYPASS CAPS



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SEMICONDUCTOR GROUP

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ENGINEER **JASON BRIDGMON**	TITLE **DDCMB**		
DRAWN BY **MARK LOVE**			
DOCUMENT CONTROL NO. **6490017**	SIZE **B**	DATE **15-AUG-2007**	REV **A**
SHEET **3** OF **3**	FILE		

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0V to 5V and the output voltage range of 0V to 5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30°C. The EVM is designed to operate properly with certain components above +50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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